EPIC Final Report

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Administrator	**San Diego Gas & Electric Company**
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Project Name	**Smart Distribution Circuit Demonstrations**
Module Name	**Module 1, Demonstrations of Advanced Circuit Concepts and Devices**
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Attribution

This comprehensive final report documents the work done in this EPIC project.

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EXECUTIVE SUMMARY

Program Objective: The objective of SDG&E's EPIC-1, Project 5, on Smart Distribution Circuit Demonstrations, was to perform pilot demonstrations of smart distribution circuit features and associated simulation work to identify best practices for integrating new and existing distribution equipment in these circuits. The project was broken into two modules:

- Demonstration of Advanced Circuit Concepts
- Demonstration of Methodologies and Tools for Energy Storage System Assessment

This executive summary describes the work and results for the first module. The work on pre-commercial demonstration of advanced circuit concepts was broadly divided into three phases:

Phase 1 included evaluation of products and technologies currently available for improved distribution circuit design, system operation, and protection. It also assessed emerging distribution circuit solutions for maintaining reliable and uninterrupted energy delivery. Hardware evaluation covered topics such as time synchronization, protection and automation control, communication, and renewables and energy storage. Some of the distribution solutions investigated include advanced distribution automation control, dynamic feeder optimization, synchrophasor-based solutions, and fault location.

Phase 2 included the selection and modeling of three distribution circuits: coastal-residential, desert-rural, and urban. The circuit parameters provided by SDG&E in Synergi Electric format were converted to RTDS Power Simulation Software (RSCAD) and validated for accuracy. A pre-commercial demonstration plan was developed to validate the distribution circuit operation and equipment performance. A hardware setup was assembled for pre-commercial demonstration of the performance of individual smart devices in a laboratory. Algorithms were developed to study system voltage coordination on distribution circuits between distributed energy resource (DER) and voltage regulators (VR). The interaction between the two device types was made possible with a controller at a central level. Circuit performance was studied during load switching via simulations. The test observations and circuit performance were captured for further analysis.

Phase 3 included the analysis of the demonstration results carried out in Phase 2 and provided recommendations on the integration and coordination of multiple voltage correction devices on a larger system, controlled by a central master controller. It is demonstrated via simulations that the DER and VR can be controlled interactively to provide voltage support on distribution circuits. Practical implementation and expansion to include other voltage correction devices are discussed. Certain modern solutions including detection of downed conductors and power quality monitoring are discussed, offering insights on how to improve the existing distribution system.

The demonstration laid groundwork for commercial adoption of the demonstrated concepts. It is recommended that SDG&E pursue commercial adoption of some of the key concepts that were demonstrated. On larger distribution circuits with multiple voltage regulation devices, system-wide voltage coordination would be required for efficient and reliable service to the customers. This implementation would also aid in improving the lifespan of various distribution equipment, as well as lowering the associated maintenance costs. Some of the challenges associated with implementing this concept in larger circuits include bringing together devices from multiple vendors on one platform and the communication protocols supported by them. Adoption of a standardized communication architecture is recommended for this purpose. It is recommended that selected devices and communications protocols be carefully evaluated before commercial adoption. A technology transfer plan was created to include the recommended steps to bridge the gap between laboratory demonstration of improved distribution practices and its successful commercial and practical implementation in the field on larger distribution circuits.

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Abbreviations and Acronyms

ACSI	abstract communication service interface
ADC	analog-to-digital converter
ANSI	American national Standards Institute
AR	automatic reconfiguration
AVR	automatic voltage regulator
BCD	binary-coded decimal
BEV	battery electric vehicle
CBC	capacitor bank controller
CES	Community Energy Storage
CT	current transformer
CVR	conservation voltage reduction
DA	Distribution Automation
DAC	Distribution Automation Controller
ADAC	Advanced Distribution Automation Control
DCLS	dc level shift
DER	distributed energy resource
df/dt	rate-of-change-of-frequency
DFO	dynamic feeder optimization
DG	distributed generator
DGA	dissolved gas analysis
DNP3	Distributed Network Protocol
DST	daylight-saving time
D-VAR	dynamic volt-ampere reactive
DVR	dynamic voltage regulator
EPIC	Electric Program Investment Charge
EV	electric vehicle
EVSE	electrical vehicle supply equipment
FFT	fast Fourier transform
FRA	frequency response analysis
FTP	File Transfer Protocol
GFCI	ground-fault circuit interrupter
GOOSE	Generic Object-Oriented Substation Event
GPS	Global Positioning System
GSE	generic substation event
GSSE	generic substation status event
GTAO	gigabit transceiver analog output
GTFPI	gigabit transceiver front-panel interface
HIF	high-impedance fault
HIL	hardware-in-the-loop
HVRT	high-voltage ride-through
ICE	internal combustion engine
IEC	International Electrotechnical Commission
IED	intelligent electronic device
IEEE	Institute of Electrical and Electronics Engineers
IFRA	impulse frequency response analysis
IGBT	insulated-gate bipolar transistor
IIR	infinite impulse response
I/O	input/output
IP	Internet Protocol
IRIG-B	Inter-Range Instrumentation Group time code format B
ISM	industrial, scientific, and medical
ISO	International Organization for Standardization
KVAR	kilovolt-ampere reactive
LAN	local-area network
LED	light-emitting diode
LTC	load tap changer
LVRT	low-voltage ride-through
MAC	medium access control
ME	multiended
MMS	manufacturing message specification
NC	normally closed
NEC	National Electric Code
NO	normally open
NTP	Network Time Protocol
OCPP	Open Charge Point Protocol
OF	overfrequency
OLE	object linking and embedding
OLTC	on-load tap changer
OPC	OLE for Process Control
OSI	Open System Interface
OV	overvoltage
P	active power
PCC	point of common coupling
PCS	Power Conversion System
PDC	phasor data concentrator
PHEV	plug-in hybrid electric vehicle

PHY	physical layer
PID	proportional integral derivative
PLC	programmable logic controller
PMU	phasor measurement unit
ppm	parts per million
PT	potential transformer
PTP	Precision Time Protocol
pu	per unit
PV	photovoltaic
Q	reactive power
rms	root-mean-square
RSCAD	RTDS Power Simulation Software
RTAC	Real-Time Automation Controller
RTD	resistance temperature detector
RTDS	Real Time Digital Simulator
RTN	return-to-normal
RTU	remote terminal unit
SAE	Society of Automotive Engineers
SCADA	supervisory control and data acquisition
SDG&E	San Diego Gas & Electric Company
SDI	sum of difference current
SE	single ended
SER	Sequential Events Recorder
SFRA	sweep frequency response analysis
SMV	sampled measured value
SNTP	Simple Network Time Protocol
SOE	Sequence of Events
SOTF	switch onto fault
TCP	Transmission Control Protocol
THD	total harmonic distortion
THDI	total harmonic distortion, aggregated current
THDV	total harmonic distortion, aggregated voltage
TOD	time of day
TWFL	traveling-wave fault location
UCA	Utility Communications Architecture
UDP	User Datagram Protocol
UF	underfrequency
UL	Underwriters Laboratories
U.S.	United States
UTC	Coordinated Universal Time
UV	undervoltage
VAR	volt-ampere reactive
VFD	variable-frequency drive
VR	voltage regulator
VT	voltage transformer
WAN	wide-area network
WEP	Wired Equivalent Privacy
WiMAX	Worldwide Interoperability for Microwave Access
WPA	Wireless Protected Access
WPAN	Wireless Personal Area Network

1 INTRODUCTION

The objective of SDG&E's EPIC-1, Project 5, on Smart Distribution Circuit Demonstrations, was to perform pilot demonstrations of smart distribution circuit features and associated simulation work to identify best practices for integrating new and existing distribution equipment in these circuits. The project was broken into two modules:

- Demonstration of Advanced Circuit Concepts
- Demonstration of Methodologies and Tools for Energy Storage System Assessment

This report describes the work and results for the first module on pre-commercial demonstration of advanced circuit concepts.

The focus of this project module was to perform pilot demonstrations of smart distribution circuit features in a laboratory for a set of selected test circuits. Using simulations and hardware-in-the-loop (HIL) testing, the desired features and upgrades were tested in the selected circuits to assess their suitability for widespread adoption.

The test circuits studied in this project include:

- Coastal-residential
- Urban
- Desert-rural

This report is divided into the following sections:

- Hardware and Circuit Evaluation: This section includes documentation and evaluation of products and technologies available for improved circuit design, system operation, and protection.
- Solutions Evaluation: This section assesses emerging distribution circuit solutions and operational practices for maintaining reliable and uninterrupted energy delivery.
- RTDS Modeling: This section outlines the process involved in the modeling of circuits. The data, which includes the load, line, source, and other devices connected to the circuits, were provided in the format used by Synergi Electric, which was converted to RSCAD and validated for accuracy.
- Voltage Regulator Tests: This section describes the hardware setup for the voltage regulation operation with the test settings and procedures described in detail. Real Time Digital Simulator (RTDS) tests were carried out and recommendations are made based on the observations recorded.
- Capacitor Bank Controller Tests: The automatic capacitor controller application was evaluated to determine the best times to switch the capacitor bank in or out, based on the load and voltage profiles provided by SDG&E. This section describes the hardware setup of the capacitor bank controller and the RTDS modeling of the device. Tests were carried out on the RTDS and the observations and results recorded.
- High-Impedance Fault Detection: This section describes the hardware setup of a high-impedance fault detector, including settings involved in the high-impedance fault protection of a circuit. The high-impedance fault logic was tested for scenarios involving different fault impedances, fault locations, and responses during the load profile run.
- Power Quality in Islands: System parameters, such as voltage and frequency, were observed on pre- and post-islanded scenarios in a test circuit. This section describes the synchrophasor devices used to tabulate the results for power quality tests and their interface with the RTDS.

- Voltage Support Coordination Tests: This section describes tests that were performed on the selected test circuit to study the system response and participation of the distributed energy resource (DER) and voltage regulator (VR) in regulating the system voltage. Both devices were designed in the RTDS and master controller logic was developed to control the coordination of these voltage regulation devices. The section further describes the observations and results of the DER tests.
- Findings: This section analyzes the results of the pre-commercial demonstrations performed and provides recommendations based on the analyses. The analysis performed provides inputs for improving the existing circuits for better reliability and operability.
- Recommendations: Recommendations are provided on the integration and coordination of multiple voltage-correction devices on a larger distribution system, controlled via a central master controller. Certain modern concepts are also discussed, offering insights on how to improve the existing distribution system.
- Technology Transfer Plan: This section lays out the steps for commercial adoption of the best practices discussed in this report. The technology transfer plan describes the activities, equipment, resources involved and the required coordination between diverse groups to successfully implement the best practices commercially.

2 PROJECT SCOPE AND APPROACH

The goal of this project is to perform pilot demonstrations of smart distribution circuit features and associated simulations to analyze and identify best practices for integrating new and existing distribution equipment in a set of selected circuits. Using simulations and hardware testing, the desired features and upgrades are tested in the selected distribution circuits to assess their suitability for widespread adoption.

The following approach was adopted for successful completion of this project.

2.1 PROJECT INITIATION MEETING

A project initiation meeting was set up with the SDG&E stakeholders and the project team to review and finalize plans for the project including objectives, approach, deliverables, contractor staff, and existing SDG&E distribution design practices. The project was divided into three separate phases, interlinked to successfully achieve the tasks defined in the scope.

2.2 PHASE 1 HARDWARE AND CIRCUIT EVALUATION

Phase 1 includes the research, evaluation, and documentation of products and technologies available for improved distribution circuit design. It also includes selection of three SDG&E test circuits. Phase 1 is further divided into the following sub-tasks:

a. Identify, evaluate, and document existing products and technologies available for improved distribution circuit design, system operation, and protection. This includes diverse topics such as time synchronization, protection, automation and control, communication, and renewables and energy storage.

b. Assess and document emerging distribution circuit solutions for maintaining reliable and uninterrupted energy delivery. This includes topics such as advanced distribution automation control, synchrophasor-based applications, fault location, high-impedance fault detection, and dynamic line rating.

c. Select three different test circuits: coastal, desert-rural, and urban-residential.

2.3 PHASE 2 CIRCUIT SIMULATION AND TESTING EVALUATION

Phase 2 includes the following sub-tasks:

a. Convert the selected test circuits from Synergi Electric format into RSCAD and validate for accuracy. Hardware test racks were set up at the test facility.

b. Develop test plans to perform individual devices tests for voltage regulator, capacitor bank controllers, high-impedance fault detection, and power quality in islands.

c. Develop algorithms and a central controller-based system to perform system voltage coordination on distribution circuits between multiple voltage support devices, and the subsequent demonstration using RTDS. Additionally, recording test observations and results for all RTDS tests for further analysis.

2.4 PHASE 3 SMART CIRCUIT ANALYSIS AND RECOMMENDATIONS

Phase 3 includes the following sub-tasks:

a. Describe important findings from the circuit demonstrations.

b. Document possible enhancements to existing distribution circuits for improved circuit design and system operation.

c. Provide recommendations on the integration and coordination of multiple voltage correction devices on a larger distribution circuit, controlled via a central master controller.

d. Create a technology transfer plan to bridge the gap between the laboratory demonstration of improved distribution practices and its successful commercial and practical implementation in the field on larger distribution circuits.

e. Discuss modern solutions to improve the operational capabilities of existing distribution circuits.

2.5 PROJECT DELIVERABLES

The project deliverables were defined at the time of the project initiation meeting. The following list includes the project deliverables that were shared with the entire team for review and feedback at the task completion.

- Functional Design Specification – Describes the project scope and approach.
- Phase 1 interim report – At the completion of Phase 1.
- Phase 2 interim report – At the completion of Phase 2.
- Phase 3 interim report – At the completion of Phase 3.
- Real Time Digital Simulator (RTDS) test plans.
- Technology transfer plan.
- Final report – A comprehensive version of the above-mentioned deliverables.
- Selected circuits simplified one-line diagrams, and load and line sheets used for transferring data from Synergi Electric to RSCAD for the three selected circuits.
- RTDS models – Draft, RunTime, and load scheduler modules were used for the following three circuits modeled in RSCAD:
  - Coastal-residential
  - Urban
  - Desert-rural
- Project initiation meeting presentation.
- Phase 1 stakeholder presentation.
- Phase 2 stakeholder presentation.
- Phase 2 additional test results presentation.
- Phase 3/Final stakeholder presentation.
- Weekly/bi-weekly meeting minutes.

Bi-weekly meetings were conducted between the project teams to discuss the progress and concerns, if any. Face-to-face meetings were conducted at the end of each phase with SDG&E stakeholders and the project team members to review the completed tasks and discuss the remainder of the plan.

3 HARDWARE AND CIRCUIT EVALUATION

This section includes documentation and evaluation of products and technologies currently available for improved distribution circuit and design, system operation and protection. The broad discussion of available products in this section provides groundwork for the pre-commercial demonstrations in this project.

Note: Appendix E - Proprietary Information includes a look-up table for the vendors referred to in this report.

3.1 TIME SYNCHRONIZATION

Standard clock time is inherently inaccurate and presents added complexity in a distributed system in which several devices require precise synchronization with global time. Several protocols have been developed to control and monitor system time as the need for precise synchronization has increased across industries. The following protocols will be discussed:

- Network Time Protocol
- Simple Network Time Protocol
- Inter-Range Instrumentation Group time code format B
- Precision Time Protocol

3.1.1 Network Time Protocol

Network Time Protocol (NTP) synchronizes time across an internet protocol (IP) network. It uses Port 123 as source and destination, and runs over the User Datagram Protocol (UDP). The NTP network generally uses a time source device attached to the main time server that distributes time across the network. NTP works well over local-area networks (LANs) and wide-area networks (WANs). It requires little hardware and provides accuracies typically within a millisecond on LANs and a few milliseconds on WANs. NTP configurations typically use multiple redundant servers and diverse network paths to achieve accuracy and reliability. No more than one NTP transaction per minute is necessary to achieve a 1-millisecond synchronization on a LAN. For larger systems, NTP can routinely achieve 10-millisecond synchronization. Many NTP clients run on non-real-time operating systems such as Windows or Linux. On the Windows operating system, clock corrections of 10 to 50 milliseconds are common because the system is performing tasks deemed more important than time-keeping. Therefore, accuracy cannot be guaranteed.

3.1.2 Simple Network Time Protocol

Some devices support only Simple Network Time Protocol (SNTP), which is a simplified, client-only version of NTP. SNTP-enabled devices cannot be used to provide time to other devices; they can receive time only from NTP servers. The SNTP-enabled devices can achieve synchronization levels within 100 milliseconds.

3.1.3 IRIG-B Protocol

The Inter-Range Instrumentation Group time code format B (IRIG-B) was developed by the Inter-Range Instrumentation Group, which is the standards body of the Range Commanders Council of the United States (U.S.) military. The latest version of the IRIG-B standard was published in 2004. IRIG-B has a pulse rate of 100 per second with an index count of 10 milliseconds over its 1-second time frame. It contains time-of-year and year information in a binary-coded decimal (BCD) format, and seconds-of-day information in straight binary seconds. IRIG-B can achieve accuracy in the range of 1 to 10 microseconds.

Year information was not specified in the IRIG-B standard before the 2004 revision. The Institute of Electrical and Electronics Engineers (IEEE) previously adopted a standard (IEEE 1344, IEEE Standard for Synchrophasors for Power Systems) that included year data as part of the IRIG-B signal. This variation came to be known as IEEE 1344 extensions.

IEEE 1344 extensions use extra bits of the control functions portion of the IRIG-B time code. Within this portion of the time code, bits are designated for additional features, including:

- Calendar year (BCDYEAR)
- Leap seconds and leap seconds pending
- Daylight-saving time (DST) and DST pending
- Local time offset
- Time quality
- Parity
- Position identifiers

To use these bits of information, power system devices and other equipment receiving the time code must be able to decode them.

An IRIG-B time signal can be modulated (over a carrier signal) or unmodulated (no carrier signal), also known as dc level shift (DCLS) in the IRIG-B standard. In some manufacturers' literature, the term "demodulated" is used to describe a DCLS. However, in most cases it may be assumed the term is synonymous with unmodulated.

The IRIG-B protocol would appear the better choice, offering accuracy of 1 to 10 microseconds. Because IRIG-B systems use dedicated coaxial timing cabling between dedicated hardware clocks, the system has disadvantages. Most notable are the added expense of additional hardware and the increased time skew because of the additional physical infrastructure.

3.1.4 Precision Time Protocol

Since IEEE 1588-2008, the IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems was established, Precision Time Protocol (PTP) has addressed the clock synchronization requirements of measurement and control systems by improving accuracy and reducing cost. Among the advantages of PTP is the protocol's use of the most readily available means for network connectivity: IP over Ethernet. Taking advantage of existing Ethernet infrastructure allows considerable reuse of in-place hardware and cabling, helping reduce costs for the physical layer. PTP eliminates Ethernet latency and jitter issues through hardware time-stamping to cancel out a measured delay between nodes at the physical layer of the network. Accuracy in the range of 10 to 100 nanoseconds can be achieved with this protocol.

IEEE 1588 specifies a protocol to synchronize independent clocks running on separate nodes of a distributed control system to a high degree of accuracy and precision. The clocks communicate with each other over a communications network. In its basic form, the protocol is intended to be administration free. The protocol generates a master-slave relationship among clocks in the system by determining which of the possible sources has the better accuracy. All clocks ultimately derive their time from a clock known as the grandmaster clock. Once all clocks in a control system are synchronized, events monitored in the control system can be time stamped to a very high degree of accuracy.

3.1.5 Applications

Most relays and devices used in the power system network typically support NTP, SNTP, and IRIG-B. PTP implementation in power system devices is at a relatively nascent stage, and most of them do not support the protocol. For applications in which time-stamping is critical, IRIG-B is preferable. For applications in which cost is a factor and time-stamping with microsecond accuracy is not a factor (e.g., data storage in a distribution system), NTP/SNTP may be used.

3.2 PROTECTION, AUTOMATION, AND CONTROL

3.2.1 Dynamic Voltage Controller

In the wake of an increased global demand for energy and the realization of the harmful effects (and scarcity) of fossil fuels, there have been advances in renewable energy technology. The steady increase in the amount of photovoltaic power stations and wind farms around the world is testament to the growth of renewable energy as a paradigm shift from the use of fossil fuels. However, renewable energy is still an emerging technology and is not free of issues. One such issue with several grid-tied renewable energy sources is the impact on power quality and system operation.

In an ideal world, power distribution companies should provide customers with a smooth sinusoidal voltage with a fixed amplitude and frequency. Unfortunately, the output power for most renewable energy sources is highly variable; wind generators can produce rated power only when the wind is blowing and the efficiency of photovoltaic solar installations are affected by the presence of clouds. These variations associated with these energy sources result in voltage fluctuations and decreases the power quality of the overall system.

In addition to grid-tied renewable energy sources, the rise of non-linear loads causes voltage sags, swells, and surges on utility lines that affect power quality. Of these voltage disturbances, voltage sags most commonly affect power quality. Voltage sags can cause damage to industrial devices such as variable-frequency drives (VFDs), robotics, controller power supplies, and control relays. Fortunately, these issues associated with voltage stability and power quality can be alleviated with proper voltage regulation.

The dynamic voltage regulator (DVR) is the most effective device for voltage regulation and improved power quality in a system. The DVR is a series compensator used to mitigate voltage sags and to restore the load voltage to its rated value. It is normally installed in a distribution system between the supply and a critical load feeder at the point of common coupling (PCC). Its primary function is to boost the load-side voltage in the event of a voltage sag to avoid power disruption to the load. The DVR can also have features such as line voltage harmonics compensation, reduction of transients in voltage, and fault current limitations.

The DVR is a power electronic converter-based device capable of protecting sensitive loads from most supply-side disturbances. The general configuration of a DVR is shown in Figure 3.1 [1].

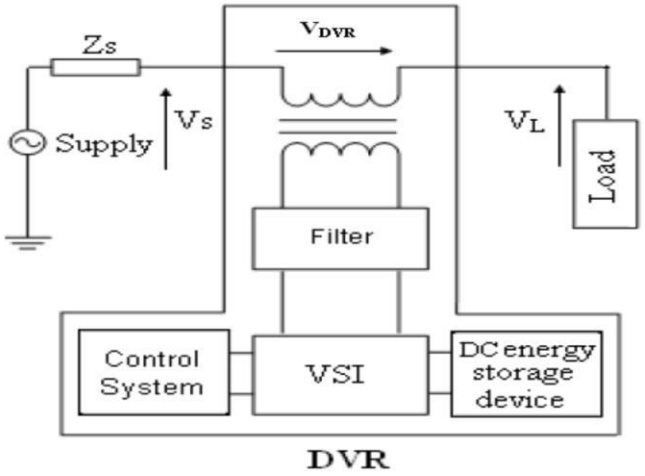


Figure 3.1: DVR General Configuration

3.2.1.1 MODES OF OPERATION

The DVR has three modes of operation:

2. Protection mode
3. Standby mode
4. Injection/Boost mode

3.2.1.1.1 PROTECTION MODE

If the current on the load side exceeds a permissible limit because of a short circuit on the load side or a large inrush current, the DVR will be isolated from the system by using bypass switches as shown in Figure 3.2 [1]. Switches S2 and S3 will open and S1 will be closed to provide an alternative path for the load current to flow.

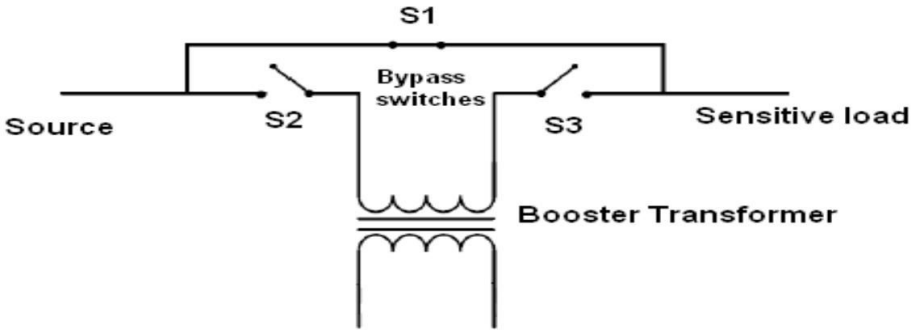


Figure 3.2: Protection Mode

3.2.1.1.2 STANDBY MODE

In Standby mode, the low-voltage winding on the booster transformer is shorted through the converter as shown in Figure 3.3 [1]. No switching of semiconductors occurs in this mode, and the full-load current will pass through the transformer primary.

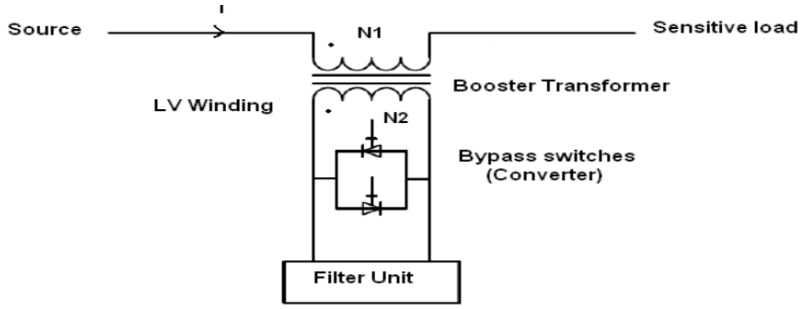


Figure 3.3: Standby Mode

3.2.1.1.3 INJECTION/BOOST MODE

In Injection/Boost mode, the DVR injects a compensating voltage through the booster transformer after the detection of a disturbance in the supply voltage.

3.2.1.2 DVR VOLTAGE INJECTION METHODS

The four methods of DVR voltage injection are discussed below. The choice of method depends on several limiting factors such as DVR power rating, load conditions, and voltage sag type.

- Pre-sag/dip compensation method: Tracks the supply voltage continuously for disturbances. If a disturbance is detected, the DVR will inject the difference in voltage between the voltage sag and the ideal prefault condition. The active power injected by the DVR cannot be controlled and is determined by external conditions such as the type of fault and load conditions.
- In-phase compensation method: The injected voltage is in phase with the point-of-contact voltage regardless of the load current and prefault voltage. The phase angles of the pre-sag and load voltage are different; however, attention is placed on maintaining a constant voltage magnitude on the load.
- In-phase advanced compensation method: Reduces the real power spent by the DVR by decreasing the power angle between the sag voltage and the load current. Active power is injected into the system by the DVR during disturbances; this active power is limited to the stored energy in the dc link of the DVR. The minimization of injected energy is achieved by making the injection voltage phasor perpendicular to the load current phasor.
- Voltage tolerance method: Voltage magnitude variations between 90 percent and 100 percent of the nominal voltage and phase angle variations between 5 percent and 10 percent of the normal state will not disturb the operation characteristics of loads. This method helps maintain the load voltage within the tolerance area with small changes in voltage magnitude.

3.2.1.3 DYNAMIC VOLT-AMPERE REACTIVE COMPENSATION SOLUTION

Vendor A dynamic volt-ampere reactive (D-VAR) was found to be a cost-effective way to provide continuous voltage regulation, improve voltage stability, meet interconnection requirements, and dynamically provide grid support where it is needed.

The main features of the D-VAR system include:

- High-speed response to voltage disturbances: D-VAR systems stabilize and regulate voltage and power factors on transmission and distribution networks and at industrial operations. The system detects and

rapidly compensates for voltage disturbances by injecting leading or lagging reactive power at key points on transmission and distribution grids. Each D-VAR system is tailored to meet specific customer requirements and accommodate changing grid conditions.

- Compliant with utility interconnection requirements: The D-VAR system can assist wind and solar generation plants in meeting utility interconnection requirements, including low-voltage ride-through (LVRT) and high-voltage ride-through (HVRT) regulation and power factor correction. The system helps reduce stress on equipment and extends its life by mitigating transient voltage events and by soft-switching capacitors and reactor banks with propriety and patented technology.
- Modular, scalable, compact, and flexible: D-VAR systems are highly modular and scalable by design. Each unit is compact to accommodate areas with space constraints. This allows utilities to install properly sized systems in the most effective power grid locations and quickly augment capability as demands increase.

3.2.1.4 D-VAR SYSTEM SPECIFICATIONS

The technical specifications of the D-VAR system (as listed on the datasheet) are shown in Table 3.1.

Table 3.1: Technical Specifications of the D-VAR System

Connection	Medium Voltage (up to 46 kV)
Frequency	50 or 60 Hz
Continuous rating	±2.0 to 100 s of MVAR
Transient overload rating	Three times continuous for up to 2 seconds
Response time	Subcycle
Inverter	Insulated-gate bipolar transistor (IGBT), 4 kHz switching frequency, rated at 1 MVAR, continuous duty
Output	Independent phase control
Harmonics	According to IEEE 519, IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems
System monitoring	Digital recording of system action, multiple inputs, alarms, and warning signals
Ambient temperature	–50°C to +50°C
Other features	– Mobile configuration for quick deployment – Minimal onsite installation – Compact installation for minimal footprint – Remote monitoring – Environmentally benign – Ambient air cooling – Robust operation during low-voltage conditions – Steady-state negative-sequence current injection to mitigate voltage unbalance

3.2.2 SCADA Capacitor

Many renewable energy systems (such as solar and wind) use dc-to-ac converters for electrical grid interconnections. During the dc-to-ac conversion, an inverter produces harmonics because of switching and a non-ideal power factor. Typically, a utility installs a capacitor bank on a distribution system for voltage and VAR support. The steps of the capacitors are automatically energized and de-energized with vacuum switches to regulate voltage, power factor, or VARs on distribution substations ranging in voltages from 4.16 kV to 34.5 kV. The banks are shipped fully assembled and ready for interconnection. All switching devices (including air-disconnect switches) and protection and control features are packaged into a single unit to allow for direct connection to the main bus of a distribution substation.

A SCADA-controlled bank offers the same benefits as conventional metal-enclosed banks; however, it goes one step further and allows for connection to a SCADA system. These SCADA-controlled banks provide the following key benefits [2]:

- Overrides automatic controls of the bank to provide voltage or VAR support to the distribution, subtransmission, and transmission systems.
- Alerts utility personnel of capacitor and fuse failures (this helps improve capacitor bank reliability).
- Reduces operating cost by reducing crew trips to the substation.
- Provides capability for remote monitoring of the status of all protection and control devices within the bank.
- Provides capability for remote monitoring of all power system parameters (harmonic distortion, voltage, power factor, etc.) associated with the capacitor bank.

A typical block diagram of a SCADA-controlled, metal-enclosed automatic capacitor bank is shown in Figure 3.4.

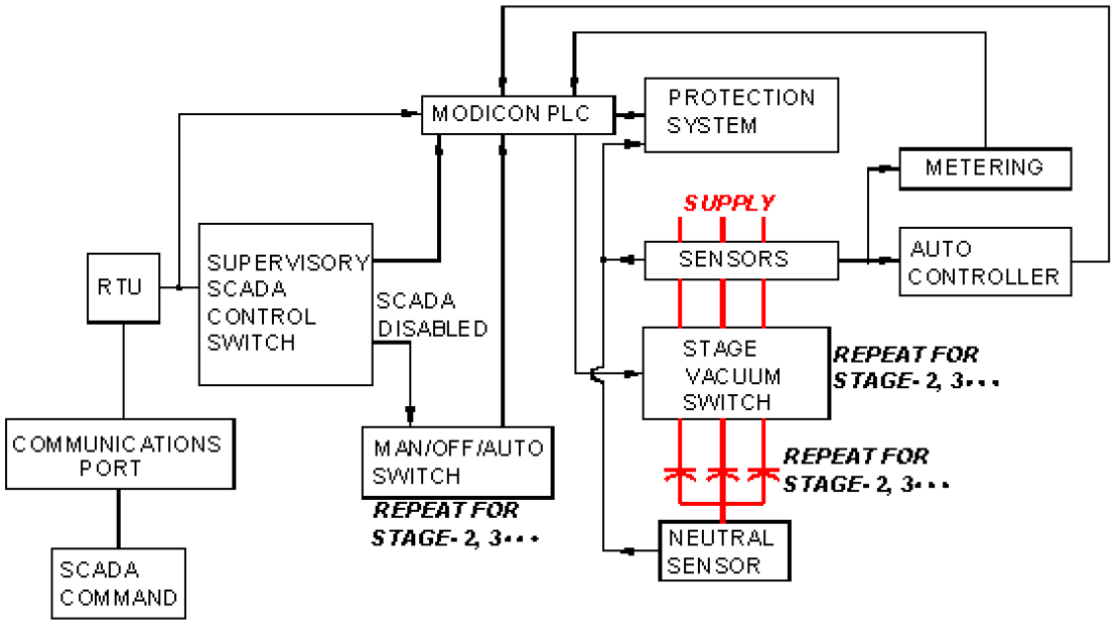


Figure 3.4: Block Diagram of a SCADA-Controlled Metal-Enclosed Automatic Capacitor Bank

The key elements in Figure 3.4 are:

- SUPERVISORY SCADA CONTROL SWITCH: This is typically located on the control panel of the metal-enclosed automatic capacitor bank. When the switch is in the Disabled position, all SCADA controls are disabled and the bank can be operated only from the control panel. The SCADA system will continue to receive indication of the capacitor bank, however, the controls received by the bank will be ignored. When the supervisory control switch is in the Enabled position, the bank can be controlled by the SCADA system, however, it will remain in Automatic Control mode until an override command is sent. Once an override command is received, the Automatic mode is disabled and complete capacitor bank control is based on commands received by the SCADA system.
- MAN/OFF/AUTO SWITCH: These are three-position switches that are functional only when the bank is not being controlled by the SCADA system. When in the ON position, the stage associated with the MAN/OFF/AUTO switch is turned on. When in the OFF position, the stage associated with the switch is turned off. When in the AUTO position, the bank is controlled by the power factor controller.
- Vendor H PLC: This controls many of the functional requirements of the SCADA control system.
- PROTECTION SYSTEM: This is composed of the neutral unbalance protection system, overcurrent relay(s), and overvoltage relay(s).
- SENSORS: These consist of the potential transformers (PTs), current transformers (CTs), and other devices required to provide SCADA and automatic control signals.
- STAGE VACUUM SWITCH: These are part of the capacitor bank and are responsible for energizing and de-energizing the capacitor bank.
- NEUTRAL SENSOR: These are located at the neutral point of most of the capacitor banks and will be either a CT or voltage transformer (VT). Their main purpose is to provide a voltage or current signal to the unbalance relay on the loss of a capacitor fuse.
- METERING: This monitors the power system parameters. These parameters are made available to the programmable logic controller (PLC) for detection of alarm and fault conditions, as well as to the remote terminal unit (RTU) for the SCADA system. A common communications protocol must exist among the RTU, metering devices, and the PLC.
- AUTO CONTROLLER: This module controls the capacitor bank stages based on system power factor, voltage, or VARs. The AUTO CONTROLLER can control the bank only if it is not being controlled by the SCADA system.

The automatic capacitor controller supported by Vendor K is a possible option for implementing SCADA capacitor controls in the system.

3.2.2.1 VENDOR K AUTOMATIC CAPACITOR CONTROLS

Vendor K supported capacitor controls are specifically designed to control pole-mounted and pad-mounted switched capacitor banks in electric distribution systems, to regulate reactive power or line voltage. With a one-way communications device installed, the capacitor controller operates in response to switching commands from SCADA or another centralized control. With a two-way communications device installed, local status information and feeder data are also available remotely, and remote configuration is possible.

With the normal standalone operation of automatic capacitor controls:

- A communications problem will not compromise VAR support.
- A problem at one capacitor bank will not affect other capacitor banks.
- Multiple contingencies are handled automatically.
- System changes and expansion do not require extensive programming.

With two-way communications equipped devices, there is no need for crews to periodically inspect the distribution capacitor banks and problems will be reported immediately. High-accuracy voltage and current inputs make it ideal for integration into advanced voltage optimization systems.

These capacitor controls offer a wide range of software-selectable functions:

- Voltage, time, temperature, time-biased voltage, and time-biased temperature control strategies.
- Voltage/temperature and SCADA override strategies.
- Automatic calculation of voltage change because of capacitor bank switching.
- Undervoltage and overvoltage protection.
- Daily limit on automatic switching operations.
- Optional neutral input sensing, which can lock out the capacitor bank if blown fuses or stuck switch poles are detected.

Other features of the capacitor controls include:

- Ease of installation: The device is available in convenient mounting types: four-jaw electric meter base, six-jaw electric meter base, pole-mounting bracket, and wall-mounting bracket. Prewired plugs are available for bracket-mounted controls, eliminating the need for field wiring. Vendor K capacitor controls accept a single-phase voltage signal from a VT, which is also used to derive control power. Models with VAR control and current control strategies also accept a single-phase current signal from a CT. When specified, the neutral input sensing feature accepts a signal from a VT, a Lindsey voltage sensor, or a current sensor.
- Ease of setup and configuration: The device can connect to a PC via USB link or an optional Wi-Fi module. Compatible software allows the operator to view real-time data, manage set points, troubleshoot problems, and download historical reports. The faceplate includes test points for the sensor inputs and a manual override switch. The system also supports remote firmware upgrades with a capable communications system.
- Extensive data access, logging, and graphing: The device provides real-time access to true root-mean-square (rms) line voltages and currents, kWs, kVAs, KVARs, power factor, temperature, and harmonics.
- Extensive data logging and graphing capabilities for optimizing performance. Parameters are logged at selected intervals and can be downloaded as tables or graphs. They include:
  - Temperature, voltage, current, power factor, KVAR, kW, and neutral current/voltage. Logging intervals can be adjusted from 1 to 60 minutes, for 2 to 120 days of voltage and temperature data.
  - Time and reason for the last 14 switching events, as well as the voltage (and VARs, if applicable) before and after bank switching. Other data include date and time of the last 15 power outages.
  - Daily minimum and maximum voltages, temperatures, currents, kWs, KVARs, power factors, neutral currents/voltages (if applicable), and number of switching cycles in the last month since installation.

3.2.3 Voltage Regulator

The main function of a utility is to supply power to its customers. With ever-increasing loads, power quality has become a critical issue for automated industries and sensitive load centers. The voltage quality is the most crucial factor that affects the power quality of a system. Voltage disturbances in the form of voltage sags, swells, and harmonics can cause damage to equipment and result in huge financial losses. Of these disturbances, voltage sags are the most common. Voltage sags can cause damage to industrial devices such as VFDs, robotics, controller power supplies, and control relays. Fortunately, issues associated with voltage stability and power quality can be alleviated with proper voltage regulation.

Voltage regulation is critical to users of electrical equipment and sensitive loads. Commercial, industrial, and residential applications require consistent voltage despite load current variations caused by expanding system demand and load profile fluctuations.

A voltage regulator is used when a steady, reliable voltage is required. Medium-voltage regulators are primarily used by the electric utilities to compensate for voltage drops in the feeders and distribution systems. The most common voltage regulators used by utilities are step-voltage regulators, which are commonly known as utility automatic voltage regulators (AVRs).

3.2.3.1 BASIC OPERATION OF A STEP-VOLTAGE REGULATOR

A step-voltage regulator is similar to an autotransformer. The step-voltage regulator has a high-voltage winding and a low-voltage winding that are connected in a way to aid or oppose the respective voltages. This means the output voltage could be the sum or the difference between the high-voltage winding and the low-voltage winding, based on the way these windings are connected.

For example, if the transformer had 10,000 V applied to the primary winding and a turns ratio of 10:1, the voltage at the secondary winding would be 1,000 V. If the primary winding and the secondary winding are connected such that the secondary winding voltage is the sum of the two windings (as shown in Figure 3.5), the secondary winding would be V_S = 11,000 V. If the primary winding and the secondary winding are connected such that the secondary winding voltage is the difference of the two windings (as shown in Figure 3.6), the secondary winding would be V_S = 9,000 V.

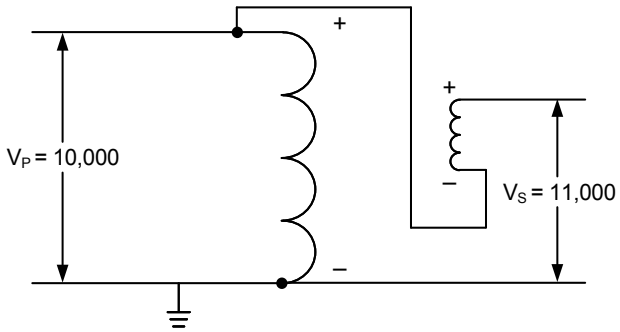


Figure 3.5: Step-Up Autotransformer (Boost Mode)

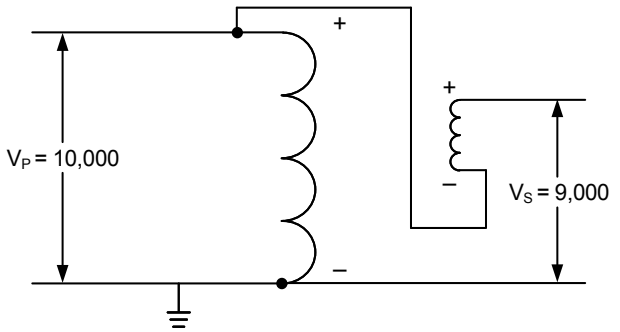


Figure 3.6: Step-Down Autotransformer (Buck Mode)

Conventional voltage regulators are the 32-step voltage regulator and the 4-step voltage regulator. The 32-step voltage regulator uses a reactor for switching and the 4-step voltage regulator uses resistors for switching. However, the basic operation of these voltage regulators is the same. The 32-step and 4-step voltage regulators are connected as shown in Figure 3.7.

This connection places the low-voltage winding on the source side of the high-voltage winding. The increase or decrease in voltage occurs ahead of the high-voltage winding. Therefore, the voltage measured across the high-voltage winding will be the final regulated voltage. In a voltage regulator, the low-voltage winding is called the series winding and the high-voltage winding is called the shunt winding. Taps can be added to the series winding for more versatility. There is an additional control winding that senses the load voltage and supplies this information to an automatic tap changer.

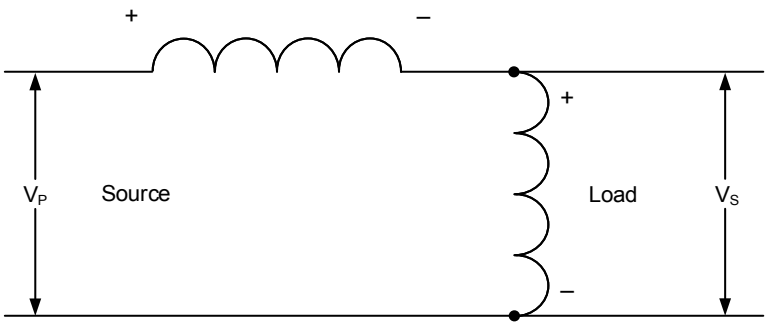


Figure 3.7: Connection of 32-Step and 4-Step Regulators

In terms of application, voltage regulators can be applied to the following circuits:

- A single-phase circuit
- One phase of a three-phase wye or delta circuit
- A three-phase, three-wire, wye or delta circuit
- A three-phase, four-wire, multigrounded wye circuit

3.2.3.2 DETERMINING VOLTAGE REGULATOR TYPE AND SIZE

The type of circuit (as previously listed) determines the type of voltage regulator to be used. However, the voltage regulator size can be determined using the circuit voltage, kVA rating, and the required amount of voltage regulation [3].

The method for calculating the required size of a voltage regulator is as follows:

1. Calculate the rated load current using the following formula:

$$I = \frac{\text{Three-phase } kVA \bullet 1{,}000}{\text{Line-to-line voltage} \bullet 1.732}$$

2. Calculate the desired voltage regulation range in kV:

$$\text{Range in kV} = \text{Voltage regulation range} \bullet \text{line-to-line voltage}$$

Note: Line-to-line voltage in kV is used for three-phase, three-wire wye or delta circuits. Line-to-neutral voltage in kV is used for three-phase, four-wire wye circuits.

3. Calculate voltage regulator rated kVA:

$$\text{Voltage regulator rated } kVA = I \bullet \text{Range in } kV$$

For example, consider a three-phase, three-wire circuit with a system voltage of 13.8 kV and a connected load of 2,000 kVA that requires a voltage correction of 10 percent. The size of the voltage regulator required for this application is calculated using the previous steps:

1. Rated load current for this application:

$$I = \frac{2{,}000 \bullet 1{,}000}{13{,}800 \bullet 1.732} = 83.7\ A$$

2. Range in voltage regulation:

$$\text{Range in } kV = 0.1 \bullet 13.8 = 1.38\ kV$$

3. Voltage regulator rated kVA:

$$\text{Voltage regulator rated } kVA = 83.7 \bullet 1.38 = 115.5\ kVA$$

For this application, a voltage regulator with a rated kVA of 115.5 should be selected.

Vendor D voltage regulator is a possible option to improve voltage quality in the system.

3.2.3.3 VENDOR D VOLTAGE REGULATOR

This single-phase step-voltage regulator is a tap-changing autotransformer that can regulate distribution line voltages from 10 percent raise to 10 percent lower in 32 steps of ⅝ percent each These voltage regulators are available from 2.4 kV to 34.5 kV for 60 Hz and 50 Hz systems.

The sealed-tank construction of the voltage regulator allows the use of a 65°C rise insulation, which provides an additional 12 percent capacity above the nameplate rating without loss of normal insulation life. The unit construction cover suspends the internal assembly for ease of inspection and maintenance. Other standard features include:

- Compliant with IEEE C57.15-2009, IEEE Standard Requirements, Terminology, and Test Code for Step-Voltage Regulators
- CL-7 control
- Tap changer with motor and power supply
- Position indicator with additional load capacity adjustment
- Two laser-etched nameplates
- Lifting lugs
- Oil drain valve and sampling device
- Upper filter press connection
- Oil sight gauge
- Mounting provisions for shunt arresters
- High-creep bushings with clamp-type connectors
- Bolt-down provisions
- Pole-type mounting brackets
- Substation base
- External series arrester
- Automatic pressure relief device
- Control cabinet with removable front panel
- Ratio correction transformer

- Conformally coated circuit boards

In addition, the voltage regulator includes a bypass arrester connected across the series winding and the load bushing. This bypass arrester helps limit the voltage developed across the series winding during switching surges, line faults, and lightning strikes.

The shunt winding can also be protected using a shunt arrester. The shunt arrester is connected between the load bushing and ground. However, a shunt arrester must be purchased as a separate accessory.

3.2.4 Reclosers

Modern power systems include reclosers along with conventional circuit breakers to provide enhanced reliability during transient events. It is a common convention to have reclosers installed at every major branch of a large power system. Because of their position in the network, they handle much less power when compared to circuit breakers at main feeders; therefore, they can trip at a lower fault threshold. This causes only a part of the system to be removed from the grid where the fault occurs. However, because of the transient nature of most faults that occur in a power system, a recloser aids in automatically reconnecting to the grid once the fault is cleared.

The most significant difference between a breaker and a recloser is that the recloser is defined as a self-controlled device. A breaker is designed for use with a separate relay/control scheme. A clear distinction between the circuit breaker and a recloser is defined in ANSI/IEEE C37.100-1981, IEEE Standard Definitions for Power Switchgear.

- Automatic circuit recloser: a self-controlled device for automatically interrupting and reclosing an alternating-current circuit, with predetermined sequence of opening and reclosing followed by resetting, hold closed, or lockout.
- Circuit breaker: a mechanical switching device capable of making, carrying, and breaking currents under normal circuit conditions and making, carrying for a specified time, and breaking currents under specified abnormal circuit conditions such as those of short circuit.

3.2.4.1 Types of Reclosers

3.2.4.1.1 Single-Phase Reclosers

Single-phase reclosers are used to protect single-phase lines, most commonly the branches or single-phase taps of a three-phase feeder system. They are also used in three-phase circuits where the load is predominantly single phase. In such applications, when a single-line-to-ground fault occurs, the faulted phase opens and locks out, while the other two-thirds of the system carries power.

3.2.4.1.2 Three-Phase Reclosers

Unlike the single-phase reclosers that operate only on one phase, the three-phase reclosers involve all three-phase contacts operating simultaneously during a trip event. There are a wide range of three-phase reclosers available, each to satisfy multiple applications at the most economical cost.

3.2.4.1.3 Triple-Single Reclosers

Triple-single reclosers combine the functionalities of single-phase and three-phase reclosers for multiple operating capabilities during faults. They have three modes of operation: three-phase trip/three-phase lockout, single-phase trip/three-phase lockout, and single-phase trip/single-phase lockout.

3.2.4.2 Recloser Controls

The recloser controls perform the calculations that help control the recloser operation. The recloser controller senses overcurrents, voltage abnormalities, recloser timing, and other recloser functions and subsequently communicates with the recloser to perform the necessary operations. There are two types of recloser controls: the internal hydraulic control and the external electronic control.

3.2.4.2.1 HYDRAULIC RECLOSER CONTROLS

The hydraulic recloser control forms an integral part of most single-phase reclosers and some three-phase reclosers. It has electromechanical controls and is mostly devoid of electronic components.

3.2.4.2.2 ELECTRONIC RECLOSER CONTROLS

Electronic controls are connected externally to the recloser and are usually housed in a separate cabinet and have electronic controls. When compared to the hydraulic controls, electronic controls are more flexible, better customized and programmed, and have increased functions such as advanced protection, metering, and automation capabilities.

The three-phase reclosers by Vendor G and advanced recloser control by Vendor L are discussed in the following sections.

3.2.4.3 VENDOR G THREE-PHASE RECLOSERS

Vendor G device is a solid dielectric, three-phase recloser controlled by an electronic recloser control The reclosers use epoxy-insulated vacuum interrupters, which provide excellent insulation while making the contacts fully shielded and void free. The reclosers are designed for three-phase automatic or manual trip operation, providing overcurrent protection for systems up to 38 kV, 800 A continuous, and 12.5 kA rms symmetrical interrupting.

3.2.4.3.1 OPERATING PRINCIPLE

Vendor G recloser consists of internal multiratio CTs and voltage sensors that monitor the circuit. The unit is powered by a 120 Vac or a 125 Vdc power source. In case of a power failure, the unit is powered using internal batteries in the control system.

The recloser has three distinct operating modes that provide maximum application flexibility:

- Three-phase trip/Three-phase lockout
- Single-phase trip/Three-phase lockout
- Single-phase trip/Single-phase lockout

The recloser control monitors the circuit parameters and controls recloser sequence operation, tripping, and overcurrent sensing functions. Each phase module consists of a magnetic actuator and a drive assembly. The magnetic actuators use permanent magnets to hold the solenoid plunger in a closed position while maintaining a charge on the opening spring. The trip/close operations are accomplished by energizing the trip coil, which generates a magnetic flux in the opposite direction and releases the trip spring. Manual trip operation is also made possible by a manual trip handle. Pulling the manual trip handle trips and locks the selected phase.

3.2.4.4 VENDOR L ADVANCED RECLOSER CONTROL

Vendor L Advanced Recloser Control is the recommended unit for the recloser. It provides the intelligence to allow reconfiguration of distribution systems and to maintain reliable service to as many subfeeders as possible in the event of a fault. The following are the features of the recloser control:

- Full line metering capabilities using voltage inputs from internal sensors.
- Six voltage inputs necessary for loop scheme designs.
- Proprietary programming for various functions such as recognizing seasonal loads and shift between Three-phase and Single-phase trip/close modes for optimal system efficiency.
- Programmable to act as a recloser for loop schemes, looking in either direction.
- Minimum trip for phase, ground, and sensitive earth faults.
- Capable of up to four shots to lockout.

- Sequence coordination.
- Harmonics up to the 15th order for total harmonic distortion (THD) analysis.
- Cold load pickup.

3.2.5 Sectionalizers

Sectionalizers provide an economical method of further improving protection of distribution lines already equipped with reclosers or circuit breakers. They are circuit-opening devices that isolate permanent faults and confine the power outage to a smaller section of the distribution system.

A sectionalizer has self-contained current-sensing transformers that power the control circuit and the circuit-opening mechanism. No auxiliary supply or external equipment or connections are required. It operates in conjunction with the source-side protection device. When the protective device de-energizes the circuit, the sectionalizer counts the number of overcurrent interruptions; when it goes beyond a preset threshold, it opens the contacts to isolate the circuit. It is not designed to interrupt fault current; therefore, it opens only during the open interval of the backup protection. Because the sectionalizer is not a time-current-based device, it can easily be added to the existing protection system without requiring a change in the coordination settings. It can be used in place of a fuse or between a fuse and a recloser.

Sectionalizers provide several advantages over fuse cutouts:

- The fault-closing capability of the sectionalizer greatly improves circuit testing after a permanent fault.
- The backup recloser can take care of power interruption if the fault is still present.
- Sectionalizers do not need replacements (contrary to fuse links). The line can be tested and service restored faster, more economically, and with more convenience.
- Sectionalizers do not open accidently under load because of a damaged link.
- Errors are eliminated in the selection of the correct fuse link size and type.

3.2.5.1 SELECTION CRITERIA

The selection of an appropriate sectionalizer is dependent on the following factors:

- System voltage: Sectionalizers are generally insensitive to the system voltage because they are not a factor upon which the device operates. However, the sole criterion to consider is that they meet the dielectric value and the appropriate voltage rating of the distribution system to which they are connected.
- Pickup current (actuating current): For reliable operation, the sectionalizer should be set to pick up current thresholds like the protective device upstream. The pickup should also be sensitive enough to register ground faults in the system, which in turn initiates automatic reclose operations.
- Inrush current restraint: One of the main causes of unwanted sectionalizer operation is inrush currents. The pickup current is a primary setting; however, depending on the position of the sectionalizer, it must be able to withstand possible transformer magnetizing inrush currents. The anti-magnetizing feature of the device ensures there is no operation if the positive and negative half cycles are below the pickup value. The inrush restraint feature thus prevents false counting and operation because of inrush currents during operation of the source-side protective device.
- Number of counts: The sectionalizers can operate for up to three recloser operation counts. For maximum reliability, the sectionalizer should be set to a count one less than the recloser upstream.
- Maximum fault current: The sectionalizer should be rated at a short-time withstand greater than or equal to the available fault current.
- Continuous current: The continuous current rating of the sectionalizer should be equal to or greater than the system load current.

- Reclaim time: The time that the memory of the sectionalizer retains prior to the counts. The duration varies with the value and duration of the fault current pulses.
- Overvoltage withstand: Sectionalizers must be able to withstand up to a 65 kA lightning surge current, as specified in IEEE C37.63, IEEE Standard Requirements for Overhead, Pad-Mounted, Dry-Vault, and Submersible Automatic Line Sectionalizers for Alternating Current Systems Up to 38 kV and IEEE C62.11, IEEE Standard for Metal-Oxide Surge Arresters for AC Power Circuits (> 1 kV).
- Load breaking: Sectionalizers are designed for dead-line operation only. Manual operation under live-line conditions will cause arcing between the contacts and can damage the device.
- Dead time: The time for a sectionalizer to drop to a safe isolating current level. To prevent the device from opening under live-load conditions, the upstream relay should have a dead-line time of not less than 0.5 seconds.

3.2.6 Transformer Monitoring and Control

Transformers are among the most expensive and critical equipment in a power system. The cost of repairing a transformer (to rectify energy not being delivered to the load because of the transformer unavailability and/or possible propagation of damages to equipment downstream of the transformer) is debilitating. It is essential that all transformer parameters be monitored for unexpected deviation from normal operating values.

Interruptions or failure of an in-service transformer usually results from dielectric breakdown, electrical faults or disturbances, winding distortion, insulation deterioration, lightning, improper maintenance, winding and magnetic hot spots, loose connections, or failure of components such as no-load tap changers or bushings. The first techniques developed for transformer monitoring were time-based monitoring solutions, which performed various offline tests to detect incipient problems. These tests could be performed only after a transformer outage or during scheduled maintenance. The time-based monitoring solutions are expensive and labor-intensive, and not entirely reliable because the monitoring is not in real time.

The present trend in the power industry is to move from time-based monitoring to a condition-based monitoring system. Condition-based monitoring can acquire and process information about a transformer in real time to determine corrective actions that may be needed to protect the transformer from overload. The following sections discuss the various aspects of condition-based monitoring of transformers.

3.2.6.1 THERMAL MONITORING

Thermal monitoring involves the development of a mathematical model that predicts the temperature profile of the power transformer using the principle of thermal analysis. The real-time temperature of the transformer is compared to the predicted operating temperature to detect abnormal operation. This is important in determining the insulation deterioration in the windings because of temperature rise. The thermal model is also used to determine the top oil temperature and the hot-spot temperature rise.

3.2.6.2 DISSOLVED GAS ANALYSIS

Gases in the transformer are produced by the degradation of transformer oil and solid insulating materials. Gases are produced at a much faster rate during electrical faults. There are three categories of faults that create gases: corona discharge, thermal heating, and arcing. By determining the quantities of hydrocarbon gases (hydrogen and carbon oxides present in the transformer), the exact fault can be detected. Table 3.2 is derived from the ANSI/IEEE C57.104-2008, IEEE Guide for the Interpretation of Gases Generated in Oil-Immersed Transformers, which gives a good account on key gas concentrations and fault types.

Table 3.2: ANSI/IEEE C57.104 Standard for Dissolved Gas Analyses

Gas Description		Key Gas Concentration (ppm)		
Name	**Composition**	**Lower Limit***	**Higher Limit****	**Potential Fault Type**
Hydrogen	H_2	150	1,000	Corona, arcing

Gas Description		Key Gas Concentration (ppm)		
Name	**Composition**	**Lower Limit***	**Higher Limit****	**Potential Fault Type**
Methane	CH_4	25	80	Sparking
Acetylene	C_2H_2	15	70	Arcing
Ethylene	C_2H_4	20	150	Severe overheating
Ethane	C_2H_6	10	35	Local overheating
Carbon monoxide	CO	500	1,000	Severe overheating
Carbon dioxide	CO_2	10,000	15,000	Severe overheating
Total combustibles	TDCG	720	4,630	Severe overheating

* As the value exceeds this limit, sample frequency should be increased with consideration given to planned outage in near term for further evaluation.

** As value exceeds this limit, removal of transformer from service should be considered.

Vendor B supports a small encapsulated DGA monitor that can provide data in real time through the analysis of the insulating oil in the transformer. Some key features of the device are:

- Operates as a standalone device or in conjunction with monitoring software.
- Functions as a hydrogen monitor or is also available as a more advanced composite gas monitor.
- Contains optional pump for situations when there is poor oil circulation.
- Includes self-testing diagnostic to monitor its own performance, ensuring the device remains accurate.
- Has alarms and closing contacts for relays and digital and analog outputs.

3.2.6.3 FREQUENCY RESPONSE ANALYSIS

When a transformer is subjected to fault currents, the mechanical structure and windings are exposed to severe stresses, resulting in winding movement and structural deformations. The frequency response analysis (FRA) is a sensitive technique for detecting deformations and movement faults. It involves measuring the impedance of the windings at low voltage for a wide range of frequencies. The two FRA methods are described in the following subsections.

3.2.6.3.1 IMPULSE FREQUENCY RESPONSE ANALYSIS

The impulse frequency response analysis (IFRA) uses a single non-periodic voltage signal as an excitation or input, which is injected into one of the available transformer terminals. This excitation induces voltages on the remaining ends of the transformer. The properties of the reflected signal depend on the structure of the transformer and therefore are used to evaluate the condition of the transformer. The frequency spectrum of the input signal and the measured output signal are obtained through a fast Fourier transform (FFT) algorithm. The ratio between the two frequency spectra is obtained for analysis.

3.2.6.3.2 SWEEP FREQUENCY RESPONSE ANALYSIS

The sweep frequency response analysis (SFRA) is like the IFRA, except in the SFRA the excitation input is a low-voltage sinusoidal input (1 to 20 V_{rms} range) that is applied to the transformer terminal in a frequency sweep (Hz to mHz range). The transfer function is obtained for analysis from the ratio of output to input signal.

The FRA technique has certain limitations that prevent it from becoming a reliable transformer monitoring technique. The main limitation involves operating the FRA tests online while the transformer is connected to the power system and delivering load. The following are the drawbacks of applying the online FRA technique:

- Measurements are performed in the presence of sinusoidal high voltage that becomes more complex considering the voltage levels, personnel and equipment safety concerns, and electric noise.

- The transformer is electrically connected to the remaining elements in the power system such as the source, load, and switches. Therefore, the measurement is the response of the whole system, further complicating the interpretation of the results.
- The possible inclusion of elements in the transformer for the FRA measurement in the network could lead to vulnerabilities that may affect the power system operation.

There are FRA devices that can be used when a transformer is offline. Table 3.3 is a comparison of the analyzers supported by Vendor I and Vendor B.

Table 3.3: Comparison of Vendor I and Vendor B FRA Devices

Description	Vendor I FRA	Vendor B FRA
Frequency range	1 Hz to 30 MHz	10 Hz to 25 MHz
Output impedance	50 Ω	50 Ω
Voltage amplitude	10 V peak-to-peak	20 V peak-to-peak
Dynamic range	> 145 dB	> 90 dB
Accuracy	±0.5 dB	±1 dB

3.2.6.4 PARTIAL DISCHARGE ANALYSIS

Partial discharge or corona is a phenomenon that involves the local electric field exceeding its threshold value, causing a partial breakdown of the surrounding medium. It is caused by factors such as the main magnetic flux, stray flux, operative voltage, residual potential, and creeping discharge. Partial discharge occurs as sharp current spikes at the transformer terminals or certain winding stress points, depending on the winding insulation and nature of the winding, and can result in degradation of the insulation surrounding it. The level of degradation can be estimated by measuring these uneven current pulses.

The development of modern microprocessor-based relays with enhanced processing capabilities makes it is possible to perform transformer monitoring and control while ensuring fault protection. These relays use the thermal-based monitoring function to compare transformer internal temperatures and loss-of-life values with predefined limits. The relays are programmed to issue a warning if these limits are exceeded.

3.2.6.5 MICROPROCESSOR-BASED TRANSFORMER MONITOR

Transformer monitor is a device that performs transformer monitoring and protection. The transformer monitor works in conjunction with a resistance temperature detector (RTD) module and other sensors in the transformer core and coil for its monitoring function. For the protection function, it uses signals from the CT and VT connected to the power transformer. Figure 3.8 shows the device connection and how it monitors the transformer parameters.

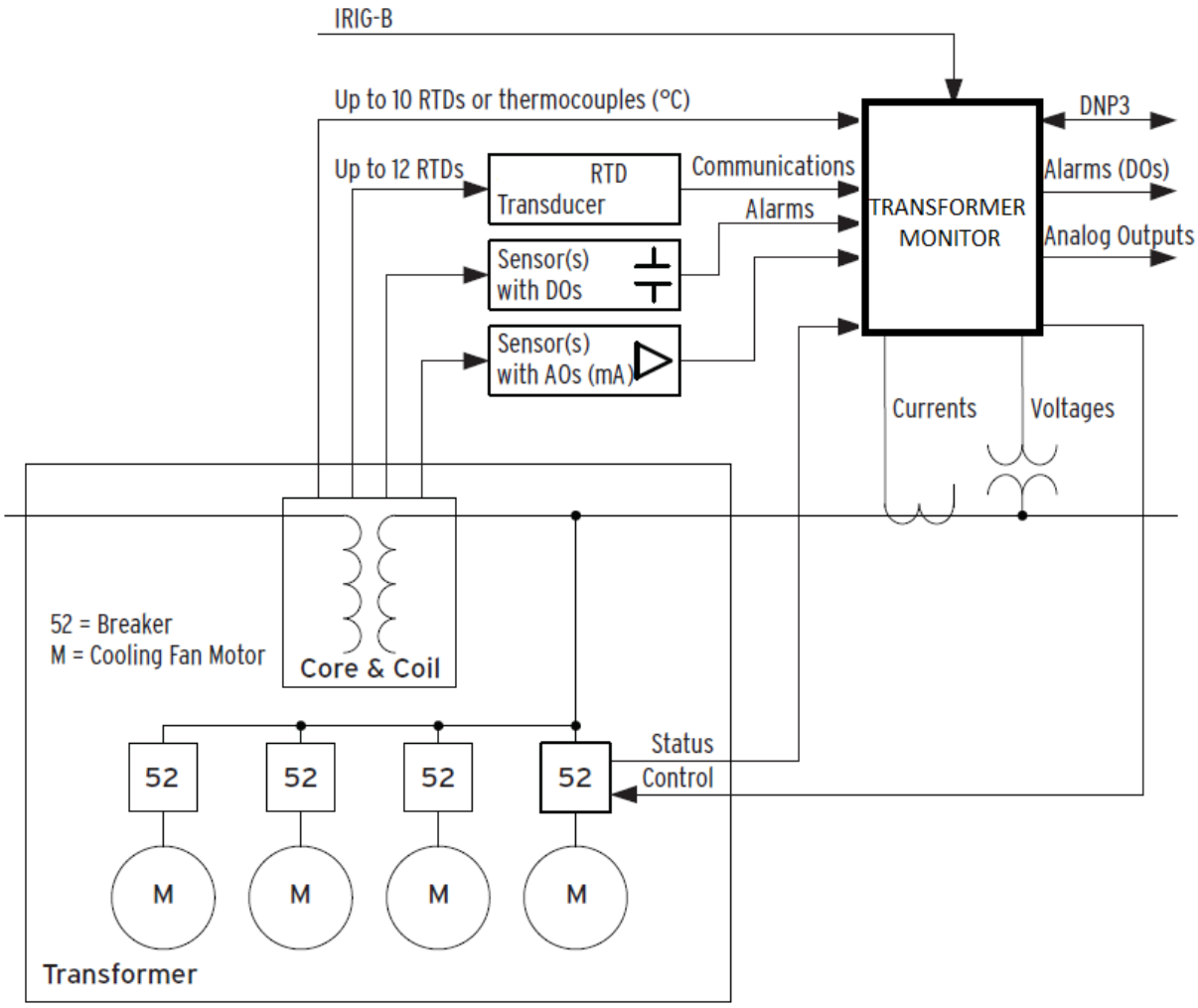


Figure 3.8: Microprocessor-Based Transformer Monitor I/O and Communications

The transformer monitor includes customizable input and output (I/O) cards that perform various functions based on the requirement. The digital inputs monitor critical transformer alarms and status points. The analog inputs measure pressure, oil level, temperature, tap position, and process-level signals (4–20 mA or 0–1 mA) from transducers. The digital and analog outputs originating from the transducers and the relay can be used to operate cooling fans, auxiliary equipment, and alarms, or provide indication. The device can also measure ac current and voltage to calculate three-phase power. In addition, it can calculate demand, generate oscillographic reports, and control automation processes (see Table 3.4).

Table 3.4: Transformer Monitor Analog and Digital I/O Monitoring Parameters

Inputs/Outputs	Status and Alarms
Digital inputs	Oil level (tank) [i]
	Oil level (conservator) [i]
	Pressure relief (tank) [i]
	Sudden pressure (Buchholz) [i]
	Gas accumulation (Buchholz) [i]

Inputs/Outputs	Status and Alarms
	Oil Flow 1 [i]
	Oil Flow 2 [i]
	Heat detector [i]
	Deluge monitor [i]
	Fan Pump 1 alarm [ii]
	Fan Pump 2 alarm [ii]
	Oil level (on-load tap changer [OLTC]) [iii]
Analog inputs	Ambient temperature [i]
	Top oil temperature [i]
	Hot-spot monitor [i]
	OLTC tank oil temperature [iii]
	Load voltage
	Load current
Digital outputs	Fan Bank 1 (on/off) [ii]
	Fan Bank 2 (on/off) [ii]
	Cooling lockout (inhibit) [ii]
	Breaker control (trip/close)
[i] Core and coil parameter [ii] Fan/pump bank parameter [iii] OLTC parameter	

In addition to the monitoring and control functions, the following are some of the features of the transformer monitor:

- Analyzes transformer Sequence of Events (SOE).
- Analyzes transformer event waveforms.
- Trends transformer temperatures and other analog inputs.
- Has through-fault event monitoring.
- Uses flexible control logic and integration features with compatibility over a wide range of communications protocols.

3.2.7 Micro-PMU

A phasor measurement unit (PMU) measures electrical waves to determine the health of the electrical distribution system using a common time source for synchronization (see Figure 3.9). Time synchronization allows synchronized real-time measurements of multiple remote points on the grid.

A PMU can be a dedicated device or can be incorporated into a protective relay or other devices. PMUs take measurements at 48 samples per second, with each measurement time-stamped to a common time reference. This allows PMUs at various locations and utilities to be synchronized.

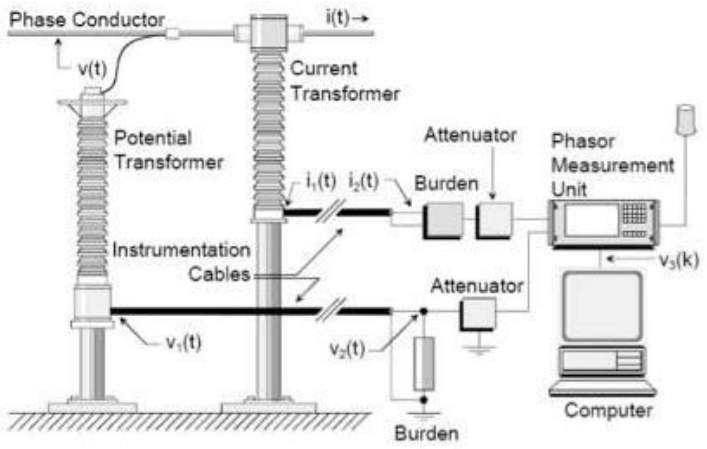


Figure 3.9: PMU Used to Monitor Power Flowing Through Electrical Grid

A single PMU cannot detect many errors in the grid. However, measuring phasors simultaneously from various PMUs at strategic locations in a system (as shown in Figure 3.10) and combining these data provides a precise and comprehensive view of the system.

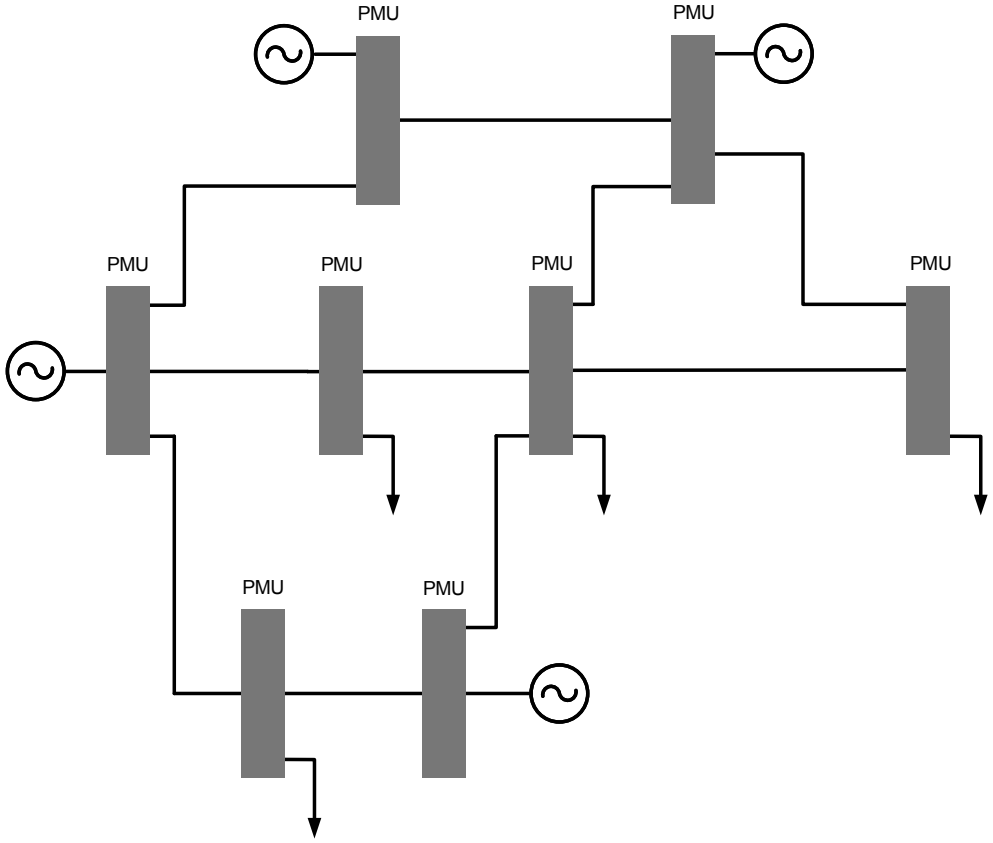


Figure 3.10: PMUs Installed at Every Substation Monitoring the Power Grid

3.2.7.1 COMPONENTS OF A PMU

From a design perspective, a PMU is a simple data collection circuit. It consists of the following components:

- A microprocessor or a microcontroller
- An analog-to-digital converter (ADC)
- A GPS receiver (to provide a precise, universal time base)
- A memory unit for storing the recorded synchrophasor data
- A communications interface to transfer the measured data back to the control room

In addition, analog inputs require a protection circuit to protect them from harmful voltages.

A simple block diagram of a PMU is shown in Figure 3.11.

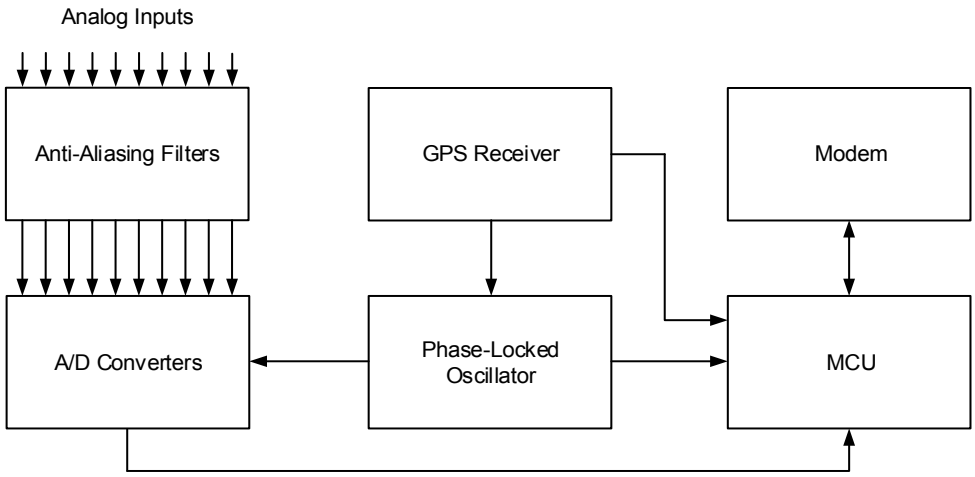


Figure 3.11: Block Diagram of a PMU

3.2.7.2 NEED FOR PMUS

3.2.7.2.1 OSCILLATION DETECTION

PMUs provide alerts to indicate levels of stress in a power grid. This stress can be in the form of low voltages, frequency oscillations, or differences in phase angles between two locations on the grid. With the increase in renewable energy generation plants connected to the grid, it is important to detect and isolate generators operating out of phase with other power stations because this can cause oscillations in the system and render the grid unstable.

3.2.7.2.2 FREQUENCY MONITORING

PMUs also help monitor the frequency in an electric power grid. Frequency fluctuates with imbalance between supply and demand of electric power. When demand is high, the frequency increases. When demand is low, the frequency decreases. If there is a rapid change in frequency, it indicates there is a loss of generation or load in the system. This kind of sudden event can cause oscillations in the grid and potentially lead to a blackout.

3.2.7.2.3 VOLTAGE STABILITY MONITORING

PMUs can help monitor, predict, and manage voltage on the transmission system of the power grid. In transmission systems, the voltage cannot exceed a certain limit without causing stability issues in the system. When voltage stability limits are exceeded, it can result in a voltage collapse.

3.2.7.2.4 DISTURBANCE DETECTION AND ALARMING

Phase angle differences between substations is a critical indicator of stress on a power system. Large phase angle differences are used for transmission operator alarms. PMUs compare the phase angles to the phase angle limits and warn the operators when stress on the system is increasing. This allows the operator to take necessary corrective measures to identify and mitigate the issue.

3.2.7.2.5 RESOURCE INTEGRATION

One of the main challenges with integrating distributed generation and renewable energy into the electric power grid is the ability to identify and respond to variability in the power generation. In a conventional system (without renewable energy), frequency is controlled by large central rotating generators. However, when more renewable energy is present in the system, it challenges the ability of the power system to control the system frequency because the change in frequency is much faster than in a conventional system. Large variations in frequency can adversely impact the stability performance of the grid. PMUs can provide real-time monitoring of frequency behavior and enable the operator to take necessary steps to maintain stability.

3.2.7.2.6 TRANSMISSION LINE DYNAMIC RATING AND CONGESTION MANAGEMENT

Dynamic rating is the ability to calculate the transmission line ratings based on environmental conditions. Typically, the ampacity of transmission lines is set at conservative values for various seasons based on a set of assumptions such as ambient temperature, wind speed, and solar heating input. However, with a combination of real-time phasor data of transmission lines and accurate local weather information, the actual ampacity of transmission lines can be calculated and would be much greater than the conservative seasonal rating. PMUs can aid in calculating the dynamic rating of transmission lines, which will help increase the throughput and relieve congestion on transmission lines.

PMUs are usually applied only at transmission systems or substations in an electric power grid. When PMUs are applied to smaller voltage levels, such as that of a distribution system, they are referred to as micro-PMUs. At the distribution level, phase angle differences are much smaller and change more rapidly than at the transmission level. This cannot be measured by traditional transmission level PMUs. Because micro-PMUs are intended to be used at the consumer voltage level, they can be created more economically, by an order of magnitude less, than the present commercial PMUs. The lower cost will allow many micro-PMUs to be deployed into the system, which will help provide a better data resolution of the distribution gird.

The micro-PMU can be connected to single-phase or three-phase secondary distribution circuits (up to 690 V line-to-line or 400 V line-to-neutral) through a PT or a standard outlet. It can also be connected to primary distribution circuits; however, the low-voltage installation is a simpler and more affordable option.

3.2.7.3 MICROPMU

The microPMU supported by Vendor J provides precise synchrophasor measurements for investigating stability and impedance issues on distribution grids and microgrids.

The microPMU measures 512 samples per nominal 50/60 Hz cycle. The measurement process adheres to IEEE C37.118, IEEE Standard for Synchrophasors for Power Systems; however, the module includes filters that are optimized for distribution and microgrid measurements. It also consists of three line-to-ground voltage measurement channels and three line current channels.

In addition, it includes 8 GB of onboard storage. This enables storage of measurements for up to 30 days.

Other features include:

- Provides up to 0.001° data resolution on voltage and current phase angles.
- Provides up to 2 parts per million (ppm) data resolution on voltage and current magnitudes.
- Supports PT connections up to 100 kV.

- Supports CT connections up to 6 kA.
- Is fully compatible with open phasor data concentrators (PDCs).
- Supports communication via Ethernet, File Transfer Protocol (FTP) file upload and download, and IEEE C37.118 streaming.
- Is able to connect to any power grid voltage with a frequency of 16.67/50/60/400 Hz and a voltage range of 100 V to 690 V, single phase or three phase.

3.3 COMMUNICATIONS

3.3.1 Communications Protocols Used in Substations

An electrical substation is a subsidiary station of the electric power system. A substation is the link between power generation and power transmission in a system. The step up of voltage for transmission or the step down of voltage for distribution and consumption takes place at an electrical substation. In addition to this critical purpose, the substation is responsible for control and monitoring of protection and power equipment, switchyard, revenue metering, and automation functions for energy management.

Substations employ protective relays and other devices to isolate system failures from affecting the entire system. SCADA systems are used to remotely monitor the status of these devices and to control system parameters when necessary. The communications protocol used by the SCADA system defines the architecture of the substation communications system.

The main task of a SCADA communications protocol is to transport digital and analog information from the substation to the control center and to allow remote control of operating parameters in the substation from the control center. The SCADA communications protocol may also be required to have the capability to access and download event files and oscillography. It should also have the ability to access devices in the substation.

The two main communications standards that have unique positions in the industry are:

- Distributed Network Protocol (DNP3)
- IEC 61850

3.3.1.1 DISTRIBUTED NETWORK PROTOCOL

DNP3 is an open and public SCADA protocol that was created by Vendor F in 1990 and is currently owned and supported by the DNP3 Users Group, which is composed of utilities and vendors who are using the protocol. DNP3 is the market leader in SCADA protocols used in the U.S.

DNP3 is based on the standards of the International Electrotechnical Commission (IEC) Technical Committee 57, Working Group 03, which has been working on an Open System Interface (OSI) Layer 3 “Enhanced Performance Architecture” protocol standard for tele-control applications. DNP3 was designed to optimize transmission of information and commands from one computer to another and is intended to be used for SCADA.

DNP3 works on serial interfaces (including RS232 and RS485), and fiber serial loop and fiber serial star configurations. DNP3 can also work over IP and Ethernet networks and is referred to as DNP3 over IP. The DNP3 protocol offers flexibility because it can be implemented over serial communication and Ethernet/IP. This allows serial devices and DNP3 over IP devices to coexist on the same network.

3.3.1.1.1 FEATURES OF DNP3

Some of the major features of DNP3 are:

- Time-stamped data
- Send and receive analog information

- Send and receive set points
- Time synchronization of data
- File download and upload capabilities
- Send and receive controls
- Report by exception (unsolicited reporting)
- Secure authentication
- Diagnostic information for each I/O point
- Communication to multiple masters
- High data integrity (no misinterpreted or corrupt data)

Being a non-proprietary standard, DNP3 has found great success in the electrical and water global sectors and has delivered significant success to the SCADA industry.

3.3.1.2 IEC 61850 STANDARD

IEC 61850 is a standard communications protocol developed by the IEC Committee 57, Working Group 10. IEC 61850 is a lower-layer, object-oriented protocol that is implemented over TCP/IP and Ethernet networks. It is based on the manufacturing message specification (MMS) that was developed by the International Organization for Standardization (ISO) Technical Committee.

More than a traditional SCADA protocol, IEC 61850 also provides information modes, abstract services, and configuration languages in substation communication.

3.3.1.2.1 FEATURES OF IEC 61850

Some of the major features of IEC 61850 are:

- Real-time information in the substation is translated into information models in the form of standard naming conventions and formats for easy information management.
- Abstract communication service interface (ACSI) allows applications and databases to remain unchanged with changes in communications protocols.
- Communications protocols are provided for TCP/IP-based SCADA, real-time Generic Object-Oriented Substation Event (GOOSE) and Generic Substation Status Event (GSSE), and real-time Sampled Measured Values (SMV).
- Substation wiring in the switchyard is reduced by converting CT and PT data into digital information.

IEC 61850 is a non-propriety communications protocol with multiple vendors that allows interoperation between devices and applications through standardized data models. It can simplify substation automation architecture with its flexible configuration of communications networks. With many vendors and customers using this communications protocol, IEC 61850 is futureproof. It can be implemented across numerous products from various manufacturers and meets a major utility requirement.

Some utilities have implemented IEC 61850 and taken advantage of an object-oriented, standardized approach to substation automation. With more vendor products that support IEC 61850 available on the market, IEC 61850 will continue to evolve.

3.3.1.3 GOOSE MESSAGING

Over the last three decades, devices in substations have evolved from electromechanical relays to digital relays with built-in communications capabilities. The advent of LAN technology has provided the capability for faster data

communication and flow of control between devices. Ethernet has become the most reliable technology for real-time applications.

IEC 61850 supports two groups of communications services between entities in a system. One group is based on the client-server model and supports services like reporting and remote switching. The other is based on the peer-to-peer model for Generic Substation Event (GSE), which provides fast and reliable communication between devices in a system and is used mainly for protection services. The GSE service also provides multicast/broadcast services, allowing the transmission of information to multiple devices.

The GSE model is divided into GOOSE and GSSE. GOOSE allows the exchange of a wide range of data organized by a data set. GSSE provides the capability to convey state-change information.

GOOSE messaging is an OSI Layer 2, broadcast/subscription Ethernet-based protocol that evolved from the Utility Communications Architecture (UCA) 2.0 GOOSE messaging protocol. This protocol is not as safe as other more common point-to-point protocols; however, it is still very useful in protection-type applications. It is particularly useful in load-shedding applications.

3.3.1.4 MODBUS

The Modbus protocol is a serial communications protocol based on the master-slave architecture. It is an open and public protocol developed by Vendor H for use with PLCs. Unlike DNP3 and IEC 61850, which are more specifically developed for applications in the power industry, Modbus is widely used across a variety of industries.

Modbus is mainly used to connect a supervisory computer to a RTU in SCADA application systems. In a standard Modbus network, there is one master unit and up to 247 slave units. Each slave unit will have a unique address. The master unit can write information to the slave units. Modbus is intended to be used as a request/reply protocol and to deliver services specified by function codes. Different versions of Modbus protocol exist for serial lines and for Ethernet applications.

One main limitation of the Modbus protocol is that it is intended to send only data and does not have the capability to send other parameters, such as point name, units, or resolution. Despite this limitation, the Modbus RTU is much easier to implement than other more modern protocols. It requires significantly lower memory than other communications protocols. With several vendor products supporting the Modbus communications protocol, it is still a dominant force in the marketplace. However, Modbus is one of the oldest communications methods and may not be a futureproof option for implementing substation automation like DNP3 and IEC 61850.

3.3.2 Implementing SCADA Over Wireless Communications Networks

Almost all substations employ SCADA systems to communicate with various intelligent electronic devices (IEDs) and other devices in the field for monitoring the system. Regular SCADA networks in substations are implemented over serial or Ethernet protocols, using copper wires or fiber-optic cables. However, copper wires and fiber-optic cables are expensive, and using them to implement SCADA in large substations will be costly and time consuming. A more cost-effective solution for implementing SCADA in large substations would be to consider implementing SCADA using wireless communications networks.

A SCADA system protocol uses polling schemes to gather information from the various devices in the field and report these data to a SCADA master. The SCADA master then makes necessary control decisions based on the information received from the devices in the field.

The polling rates of SCADA protocols can vary widely; however, typically they are not faster than once per second. The wireless communications network must account for this polling rate, protocol overhead, and number of devices in the field. To meet these requirements, the wireless communications network must have a high enough throughput. A throughput of 1 Mbps or greater will allow the wireless network to handle multiple devices regardless of the polling rate.

3.3.2.1 WIRELESS NETWORK TOPOLOGIES

There are a few network topologies to choose from when using wireless networks for SCADA applications:

- Point to point is the simplest wireless network topology. It contains only two devices. It is possible to set up multiple point-to-point networks in a single area to provide a pseudo point-to-multipoint network. However, a major drawback of this system is that if a single link in the network is compromised, it may lead to a loss in communication between the devices.
- Point to multipoint allows multiple terminal devices to communicate via a base station or access point. It allows data collection and wireless communication with multiple devices.
- Mesh allows each device to communicate with more than one device in the network. Two devices will communicate with each other directly if they are permitted to do so. Otherwise, they can use intermediary devices to relay information to each other or to a final destination. The mesh topology is a good option when devices do not have a line-of-sight to the access point. The presence of multiple links in the network ensures there will be no loss of communication if a single link is lost. However, having multiple links in the system increases the latency and lowers the throughput. Also, several devices are required to achieve path redundancy.

3.3.2.2 WIRELESS TECHNOLOGIES

This section discusses the various wireless technologies presently available on the market. Bluetooth® is based on IEEE 802.15.1, IEEE Standard for Telecommunications and Information Exchange Between Systems – LAN/MAN – Specific Requirements – Part 15. Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specification for Wireless Personal Area Networks (WPANs). It is a wireless technology intended to be used for short-range applications. Bluetooth transmission hops from one frequency to another in a predetermined manner. If data transmitted over one channel are lost, they are retransmitted at a later time over a different channel. Bluetooth is popularly used for wireless audio applications. In Electric utilities, Bluetooth has mainly been used for serial port extension over wireless for commissioning devices and collecting data regarding events.

Some of the features of Bluetooth include:

- 2.5GHz design that is accepted in both the U.S. and internationally
- Range up to 300 feet
- Bandwidth of 2.1 Mbps (depending on the application)
- Pair with utility-grade serial-to-Bluetooth adapters
- Simple plug-and-play operation and provide support for laptops, smart phones, etc.

Security concerns, limited range, and support for only point-to-point communication may limit the possible application for Bluetooth in the power industry.

3.3.2.2.1 ZIGBEE

ZigBee is a wireless technology based on IEEE 802.15.4, IEEE Standard for Local and metropolitan area networks – Part 15.4: Low-Rate Wireless Personal Area Networks (LR-WPANs). It is usually used in lighting, traffic management systems, and industrial sensors. ZigBee supports low to moderate data throughput systems. Industrial radios based on this standard can handle SCADA data collection.

Some of the features of ZigBee include:

- Operates on 900 MHz (U.S.) and 2.4 GHz (U.S. and international).
- Covers a range of 300 feet to 1 mile.
- Uses low power consumption.
- Contains a bandwidth of 1.5 MHz.
- Supports application in point-to-point, point-to-multipoint, and mesh networks.
- Supports interoperability between devices.

ZigBee has potential for numerous applications in electric utilities; however, there are limited devices that support any application in this market. ZigBee has poor security features and is not secure.

3.3.2.2.2 WI-FI

Wi-Fi is a wireless technology based on IEEE 802.11, IEEE Standard for Information technology – Telecommunications and information exchange between systems Local and Metropolitan area networks – Specific requirements Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications. It provides broadband communications access, which is desirable for industry and consumer applications. Wi-Fi devices have a link range of 300 feet and can be extended up to 1,000 yards with high-gain directional antennas.

Some of the features of Wi-Fi include:

- Operates on 2.4 GHz and 5.8 GHz (U.S. and international) industrial, scientific, and medical radio bands (ISM bands).
- Contains bandwidths of 5, 10, and 20 MHz.
- Covers a range of 300 feet (can be extended to 1,000 yards).
- Has better security options (WPA and WEP).
- Allows a higher throughput.
- Permits interoperability between devices.

Given its features, Wi-Fi represents the most promising option for implementing SCADA over wireless networks. However, it does have disadvantages. Because Wi-Fi is a popular technology used by industries and consumers, signal interference could be an issue. Although the range of Wi-Fi can be extended, it still has a limited range and its effectiveness will depend on the size of the facility or system. Another important criterion to be considered is that most Wi-Fi devices are not substation-hardened and may not meet the necessary standards required for being applied to substations.

3.3.2.2.3 WORLDWIDE INTEROPERABILITY FOR MICROWAVE ACCESS

Worldwide Interoperability for Microwave Access (WiMAX) is a group of wireless communications standards that implement IEEE 802.16, IEEE Standard for Local and metropolitan area networks Part 16: Air Interface for Broadband Wireless Access Systems, to provide up to 40 Mbps data rates. WiMAX was designed to provide high-speed broadband internet to devices over long distances.

WiMAX is often compared to Wi-Fi; however, there are key differences between them. WiMAX can provide a much wider wireless access than Wi-Fi. Unlike Wi-Fi, which is a networking technology that allows devices to connect to a network using the 2.4 GHz and 5 GHz ISM bands, WiMAX is a cellular technology that uses base stations and network infrastructure to allow devices to connect to a network. Access to the network is controlled by the base station. WiMAX supports multiple bandwidths ranging from 1.5 MHz to 28 MHz.

WiMAX gets its name from the WiMAX Forum, an industry group that promotes WiMAX use. The group was formed in 2001 and promotes conformity and interoperability.

Some of the features of WiMAX include:

- Covers a long range.
- Allows high data speeds (up to 40 Mbps).
- Contains better security (user authentication, device authentication, wireless encryption, and key management).

The major drawback of WiMAX is the cost associated with setting up base stations and network infrastructure. WiMAX is more suited to large utility systems and would not be a cost-effective choice for smaller systems.

3.4 RENEWABLES AND ENERGY STORAGE

3.4.1 Multifunction Inverters

Increases in solar power plants and distributed generation make it imperative for the grid to have infrastructure that is more intelligent and resilient to provide a stable and consistent flow of power.

The photovoltaic (PV) inverter, the basic building block of a solar power plant, could have the potential to aid the grid from being overwhelmed by the increasing number of renewable energy plants (which are mostly inverter based) connected to it. Unlike traditional inverters, a multifunction inverter (sometimes called smart inverter) has bidirectional communications capabilities and a robust software infrastructure.

A smart inverter can send and receive messages swiftly and share data with the owner and the utility. A smart inverter can be capable of the following functions:

- Connect/disconnect function. There are numerous possible reasons for disconnecting distributed devices from the grid. Unacceptable high-voltage levels, malfunctioning DER equipment, and maintenance requirements are among them. The utility can issue a "disconnect" command to disconnect DER devices from the system without loss of power to customers.
- Power factor control. Smart inverters allow control of reactive power by controlling the ratio of real power to reactive power.
- Maximum generation limit control. The smart inverter can control the real power output of a connected distributed generation device. This ensures the output from the distributed generation does not cause overvoltage conditions. This will in turn ensure devices such as transformers are not stressed by overvoltage conditions in the system.
- Intelligent volt/VAR control. The smart inverter can regulate voltage by modulating the reactive power output of the connected distributed generation device.
- Intelligent volt-real power control. Smart inverters can provide voltage regulation by modulating the real power output.
- Frequency control. Smart inverters allow DER systems to help with frequency regulation by modulating real power output.
- Power curtailment. Smart inverters can control the power output from a system by specifying an upper limit for the active power output from the system.
- Low- and high-voltage and frequency ride through. Smart inverters can adjust their output and remain connected to the grid under low- and high-voltage and low- and high-frequency conditions.

3.4.1.1 VENDOR C SOLAR INVERTER

Vendor C solar inverter incorporates PLCs, advanced VFDs, and protective relays. It has the intelligence to automate operations, commission, and shutdown procedures with minimal physical action.

This device is designed specifically for 480 Vac three-phase applications and 600 Vdc PV systems.

Some of the features and benefits include:

- Grid sensor-based vector control. Ensures precise synchronism and fast response to grid dynamics and ensures system stability.
- Advanced proportional integral derivative (PID) control. Precise synchronism to the grid enables finer current and power limits and better reactive power or power factor control.
- Large dc bus capacitors. Ensures better solar module operation with extremely low ripple current on the PV array.

- Advanced anti-islanding function. Ensures the operation of the inverter is prevented in the event of a utility outage.
- Dual storage 250 kW with hysteresis. Provides optimum efficiency in lower irradiance conditions. Improves inverter longevity with less stressful power-stage operation.
- Maximum power point. Fast response time reacts to sudden changes, improved current response for low-irradiance periods, sudden-onset shading, and grid outages.
- Remote monitoring interface. Compatible with third-party monitoring applications via Modbus/TCP with an RJ45 plug and a terminal block with additional I/O.

3.4.2 Community Energy Storage (25–100 kW)

3.4.2.1 INTRODUCTION

With the increasing presence of renewable energy generation, the need for large-scale energy storage units is indispensable. Grid-connected energy storage is essential to decrease the dependence on fossil fuel-based generation. It also helps in smoothing the variability of wind and other renewable sources of energy. Optimum integration of renewables in conjunction with grid-connected energy storage enables the power grid to better balance sources and loads while reducing carbon emissions.

Community Energy Storage (CES) systems can provide reliable local backup for communities, improve power quality, manage peak loads, and possibly improve power reliability indices. Energy storage will help reduce outages by swiftly dispatching power when grid power is unavailable. Existing industrial solutions for CES systems are discussed in the following sections.

3.4.2.2 INDUSTRIAL SOLUTIONS AND PRODUCTS

The Community Energy Storage System functions as an intelligent distributed energy storage system to help utilities meet their rapidly changing needs. By positioning discrete amounts of utility-controlled storage where required along the distribution circuit, the utilities can rapidly respond to changing electricity demand. Other applications that encourage the shift toward smart grid include: integration of renewables, managing the intermittent nature of renewable sources, managing peak loads including plug-in electric vehicles charging stations, and improving reliability indices by providing immediate backup power. High-speed transfer from grid to backup source makes the outage seem barely perceptible to customers.

Figure 3.12 shows a simplified illustration for using multiple energy storage units (CES fleet systems) to support a larger consumption. It essentially acts as a substitute for a peaking power plant. Vendor K supported Distributed Energy Management System offers the technology for smart management of multiple energy storage units. It offers the following features:

- Uses DNP3 communication
- Supports SCADA
- Allows real-time and archival data storage
- Integrates with central office systems
- Maintains system security with user authenticated login/logoff

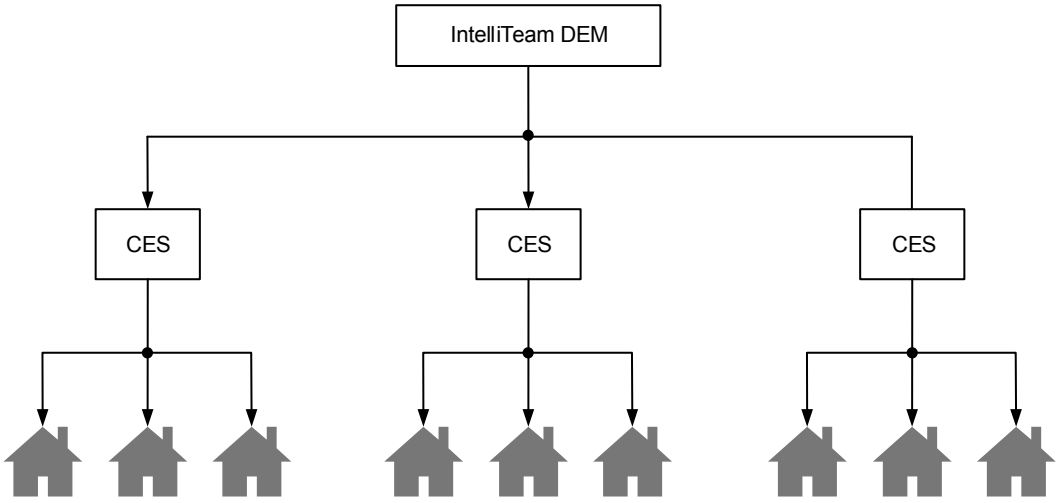


Figure 3.12: Simplified Representation of DEM Systems Supporting CES Fleet Systems

3.4.2.2.1 PHYSICAL LAYOUT

Vendor K supported CES consists of two main units as shown in Figure 3.13.

- Power Conversion System (PCS) Enclosure: Suitable for outdoor installation. It consists of an ac circuit breaker, an inverter, user-accessible ac termination area, user-accessible dc termination area, and user-accessible controls area.
  - AC circuit breaker: Automatically isolates the power unit from the utility source if the source is interrupted.
  - Inverter: If the ac circuit breaker is opened in response to interruption of the utility source, the inverter will provide the islanded load until service is resumed or energy in the battery pack is depleted.
  - DC breaker: Provides isolation of the battery pack, allowing maintenance to be performed on the PCS.
- Battery enclosure: An energy storage unit consisting of either a user-selected 25 kWh or 50 kWh lithium-ion battery pack suitable for installation underneath the PCS. The CES unit should be connected to the 120/240 Vac secondary of the outdoor utility distribution transformer at a frequency of either 50 Hz or 60 Hz.

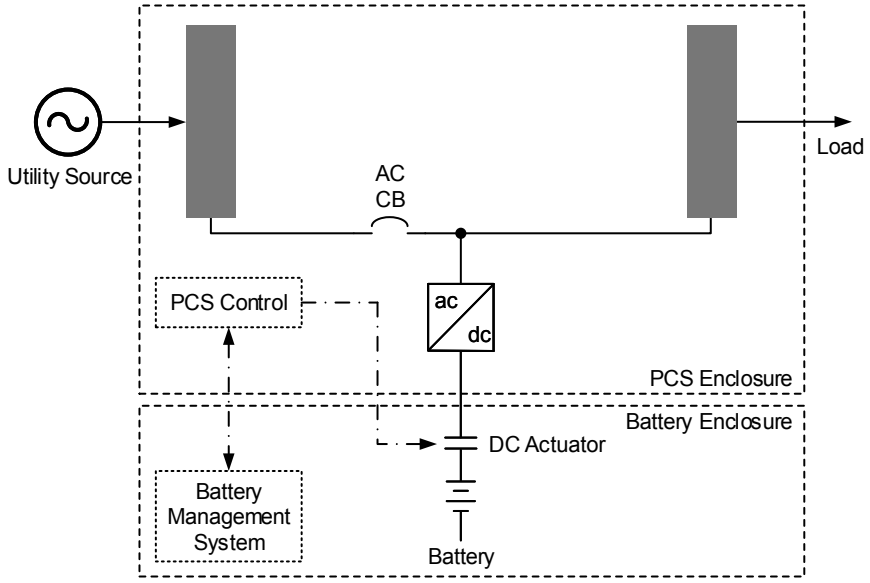


Figure 3.13: Simplified Circuit Representation of CES Units

3.4.2.2.2 OPERATIONAL PRINCIPLE

- Normal mode/utility connected: In normal operation, the CES operates in Current Source mode, providing functionalities such as voltage regulation, power factor correction, peak shaving, and load following.
- Island mode/utility disconnected: If the utility service is interrupted for any reason, the ac breaker in the unit will open, isolating and islanding the load from the utility service. The energy storage unit and inverter will then power the islanded load for a period depending on the battery bank capacity and the load. The energy storage unit will continue to support the load until utility service is resumed or the energy storage unit of the CES is depleted.

3.4.2.2.3 DEVICE MANAGEMENT

The operation, control, and monitoring of the CES can be done through the remote setup software. This program can be accessed by operators via secure Wi-Fi connection or WAN radio using a PC with compatible software. This software also works in conjunction with the IntelliTeam DEM system for CES fleet systems. The following features are offered by the IntelliLink program:

- Monitors the status of CES.
- Enables smart load management (load following function) that continuously adjusts the CES output to remain at or within the user-configured limits.
- Provides diagnostics, logging, and alarms.
- Schedules charge and discharge profiles for day of the week.
- Contains security settings.

3.4.2.2.4 RELEVANT STANDARDS COMPLIANCE

The following is a list of standards to which the CES units comply:

- IEEE 1547-2003 (R2008), IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems.
- IEEE 1547.1-2005, IEEE Standard for Conformance Test Procedures for Equipment Interconnecting Distributed Resources with Electric Power Systems.
- IEEE 1547.3-2007, IEEE Guide for Monitoring, Information Exchange, and Control of Distributed Resources Interconnected with Electric Power Systems.
- ANSI/IEEE C2-2007, National Electrical Safety Code.

3.4.3 Commercial Electric Vehicle Supply Equipment Clusters

3.4.3.1 INTRODUCTION

The electric vehicle (EV) is an automobile powered entirely or partially by electricity. Increased use of EVs provide multiple benefits, from reducing greenhouse gas emissions to minimizing dependence of petroleum. EVs are classified as follows:

- Battery electric vehicle (BEV): Propelled entirely by a battery-powered electric motor. Typically operates between 80 and 100 miles on a single charge.
- Plug-in hybrid electric vehicle (PHEV): Propelled by a combination of a battery-powered electric motor and a gas-powered internal combustion engine (ICE). It operates up to 40 miles on battery power, then switches to the ICE to propel the vehicle either directly or through the electric motor.

3.4.3.2 COMMERCIAL EVSE CLUSTERS

The electrical vehicle supply equipment (EVSE) is the electrical energy transfer device that conducts and regulates power from the electrical portal connection to the EV inlet. For EV use to become more widespread, it is required that reliable, efficient, and user-friendly infrastructure be developed. To achieve this, research in recognizing and identifying strong EVSE networks or "clusters" is essential. This identification is based on factors including the area's demographics and nature of potential EVSE location: publicly-owned or privately-owned, etc. Commercial clusters include areas like downtown, workplace, higher-education campus, leisure destinations, medical campus, and regional transit center. In a commercial setting, clustering refers to adjoining businesses that might install EVSE or multiple EVSE on one site.

3.4.3.3 CHARGING OPTIONS

According to the Society of Automotive Engineers SAE J1772TM-2011, "Standard for Electrical Connectors for Electric Vehicles," EVs can be charged via defined levels/rating of ac and dc power (see Table 3.5).

Table 3.5: SAE J1772TM-2011 Charging Configurations and Rating Terminology

Level	Rating	Estimated Charge Time
AC Level 1	120 V, 1.4 kW at 12 A	PHEV:7 hours BEV: 17 hours
	120 V, 1.9 kW at 16 A	
AC Level 2	240 V, 7.68 kW at 32 A	PHEV: 1.5 hours BEV: 3.5 hours
	240 V, 19.2 kW at 80 A	PHEV: 22 minutes BEV: 1.2 hours

Level	Rating	Estimated Charge Time
DC Level 1	200–450 V, up to 3 kW (80 A)	PHEV: 22 minutes BEV: 1.2 hours (Based on 20 kW)
DC Level 2	200–450 V, up to 90 kW (200 A)	PHEV: 10 minutes BEV: 20 minutes (Based on 45 kW)

Note: SAE J1772 is a North American standard for electrical connectors for EVs maintained by the SAE International. It covers the general physical, electrical, and communications protocols, and performance requirements for the EV conductive charge system and coupler.

3.4.3.4 ELECTRICAL ASSESSMENT OF SITE PRIOR TO INSTALLATION

Prior to implementation of an EVSE infrastructure, it is necessary to carry out a site assessment to evaluate the quantity and type of vehicles that will be charged, rate of turnover, electrical service availability, and physical space availability for charging. For this report, the focus is on electrical service assessment for a selected site. Figure 3.14 outlines the different steps for this assessment.

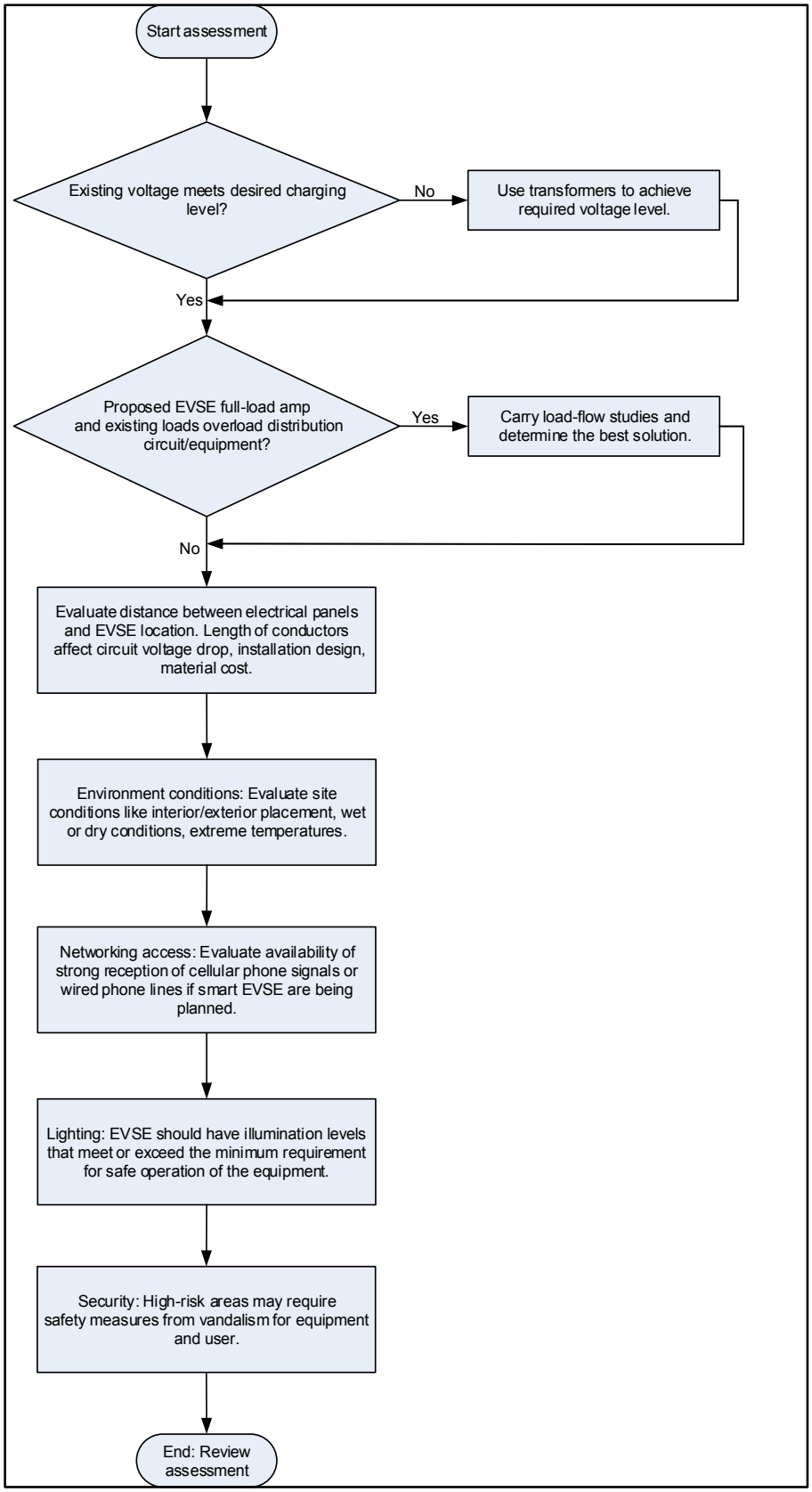


Figure 3.14: Electrical Assessment Prior to EVSE Installation

3.4.3.5 INDUSTRIAL SOLUTIONS AND PRODUCTS

EVSE are classified based on their networking capabilities as described in the following subsections.

3.4.3.5.1 BASIC EVSE

Basic EVSE, also referred to as a "Dumb" charger, communicates only with the vehicle. The handshake begins the charging process, and the process ends when the charge is complete or interrupted by the EVSE or uncoupling. A basic EVSE is simple to operate and maintain, and is generally less expensive than a smart EVSE. No other connection besides the electrical infrastructure is required. Models are available in both Level 1 and Level 2 charging, as explained in Table 3.5, and are manufactured for residential and commercial purposes.

3.4.3.5.2 SMART EVSE

The charger offers different levels of communication and networking with the end user, site host, utility grid, and the internet depending on the model type and manufacturer. It also offers the option of collecting a fee for the charging session and reporting capabilities.

Commonly available end-user features include accessibility through computers or smart phones, user verification, sales using credit cards, display of fee rates, rate of charging, cell phone or email notification of completed session, plug-out notification, internet location, availability, and reservation of EVSE with rates.

Commonly available reporting features include date, location, electricity use of each charging session, monthly reports, and fee totals. The site host can communicate with the smart EVSE to establish rates, determine usage, verify user identity, troubleshoot errors, and gather kWh consumption for analysis.

Vendor E EVSE provides 220 Vac and up to 30 A. It is designed according to the SAE J1772 requirements to meet all safety codes specified by UL and National Electric Code (NEC). The unit is engineered for commercial interior or exterior locations and comes in single, dual-wall, or pole-mounted versions. It is equipped with an automatic cable management system, which fully retracts and protects the 20-foot cable from weather-inflicted damages or vandalism.

The design is modular in nature and can be configured for simple on/off control, or provide the more sophisticated option of credit/debit and ID card processing. EVSE chargers are compatible with Open Charge Alliance charger networks. This ensures universal access to chargers without proprietary membership required. Table 3.6, documents the networking specifications.

Note: The Open Charge Alliance is an international standard for the development of charger networking based on an open versus proprietary architecture.

Table 3.6: Vendor E EVSE Networking Specification

Function	Specifications
Communications	Ethernet, cellular, and other radio communications, Wi-Fi
Networks	Web-based, LAN, WAN, cellular, Open Charge Point Protocol (OCPP)
Power monitoring	Integration with third-party monitoring systems
EV charge payment	EV charger kiosk or payment station integrated with current system

3.4.3.6 RELEVANT STANDARDS COMPLIANCE

The following are the standards to which the Vendor E EVSE units comply:

- UL 2231-1, Standard for Safety for Personnel Protection Systems for Electric Vehicle (EV) Supply Circuits: General Requirements.
- UL 2231-2, Standard for Safety for Personnel Protection Systems for Electric Vehicle (EV) Supply Circuits: Particular Requirements for Protection Devices for Use in Charging Systems.

3.4.4 Microgrid Solutions

A microgrid is a discrete energy system consisting of distributed energy sources (including demand management, storage, and generation) and loads capable of operating in parallel with, or independent from, the main power grid.

Microgrids can help reduce greenhouse gas emissions and lower stress on the transmission and distribution system by providing local, reliable, and affordable energy security for urban and rural communities while also providing solutions for commercial, industrial, and federal government consumers.

The primary driver for microgrids is the ability to deliver reliable, clean power to critical facilities during an extended period by islanding or operating independently of the utility grid. By controlling the demand and generation, dynamic stability, and optimizing control on a small scale, the microgrid can better manage the local power generation.

A microgrid connects to the grid at a PCC that maintains voltage at the same level as the main grid unless there is an issue on the grid. Microgrids can perform dynamic control over energy sources, enabling autonomous and automatic self-healing operations. Microgrids interoperate with existing power systems, information systems, and network infrastructure, and are capable of feeding power back to the larger grid during times of grid failure or power outages.

Microgrids are typically powered by renewable energy sources, diesel generator sets, fuel cells, and natural gas generators. However, PV and battery technologies are economically viable and can provide sustainable electricity and fuel growth for microgrid applications.

Some of the key features of the microgrid are:

- Operates in Island mode or Grid-connected mode.
- Connects to the main grid as a single controlled entity.
- Contains provisions to control the levels of power quality and reliability for end users.
- Accommodates total system energy requirements.
- Combines interconnected loads and co-located power generation sources.

Creating a successful microgrid is challenging. It involves understanding basic system requirements, accommodating unique operating characteristics of generation sources, managing and prioritizing power requirements, and seamlessly interfacing with the utility grid. A structured approach to microgrid implementation gives us the ability to support critical infrastructure, even in the event of a major power disruption. Extensive modeling and analysis must be performed to address the protection of the generation assets and subsystems.

Some technical challenges when implementing microgrids are:

- Management of large imbalance between load and generation.
- Use of different generation technologies.
- Presence of power electronic interfaces.
- Protection and safety for consumers and utility personnel.

Section 3 provides research and evaluation of products and technologies available for improved circuit performance and reliability. Products supported by a variety of vendors were considered for this analysis. This section aims at providing the groundwork for the options available for improved distribution circuits, to the reader. It also documents the basic features of the devices shortlisted and used in the demonstration of advanced circuits concepts through laboratory simulations.

4 SOLUTIONS EVALUATION

This section assesses emerging distribution circuit solutions and operation practices for maintaining reliable and uninterrupted energy delivery. It also highlights the baseline data which is used to understand the system characteristics under normal and abnormal conditions.

4.1 ADVANCED DISTRIBUTION AUTOMATION CONTROL

The Advanced Distribution Automation Control (ADAC) consists of a Distribution Automation Controller (DAC) that communicates with switch controls, recloser controls, feeder relays, and other IEDs.

The two main control objectives addressed by a ADAC are:

1. Automatic reconfiguration: Including or excluding a feeder from a scheme based on the evaluation of events by the ADAC.

2. Dynamic feeder optimization: Involves the continuous monitoring and control of tap-changing equipment and reactive power sources in the distribution system to improve voltage profiles and provide power factor correction.

The ADAC performs many functions, such as:

- Detecting open-phase and permanent fault conditions on the network and taking necessary steps to isolate the affected zone and restore power to the area.
- Detecting overload conditions in a system and taking necessary steps to mitigate effects by transferring load to adjacent feeders.
- Detecting loss-of-source and station events and taking necessary steps to isolate the event.
- Optimizing the operation of the distribution network by controlling voltage regulators and capacitors to improve the voltage profile and control power factor.
- Detecting the falling conductor.

The ADAC is implemented using a Real-Time Automation Controller (RTAC). The serial communications ports on the DAC are used to connect to reclosers, feeder relays, etc., to implement the required ADAC architecture. The DAC collects data and communicates with other IEDs using the DNP3 protocol. Each connected device is polled by the ADAC to ensure the device is healthy. The usual control commands sent by the ADAC include open and close commands, reset commands, and commands to change the settings group. More commands can be sent by the ADAC based on the way it is configured and the way it is connected to the external system.

Figure 4.1 shows a simple arrangement in which a ADAC is implemented using an automation controller that communicates with two relays via an RTU. The RTU is connected to serial communication Port 2 of the automation controller. These relays will, in turn, control the operation of circuit breakers in the system. Serial communications Port 1 is connected to a relay via radio. Serial communications Port 5 is used to communicate with SCADA.

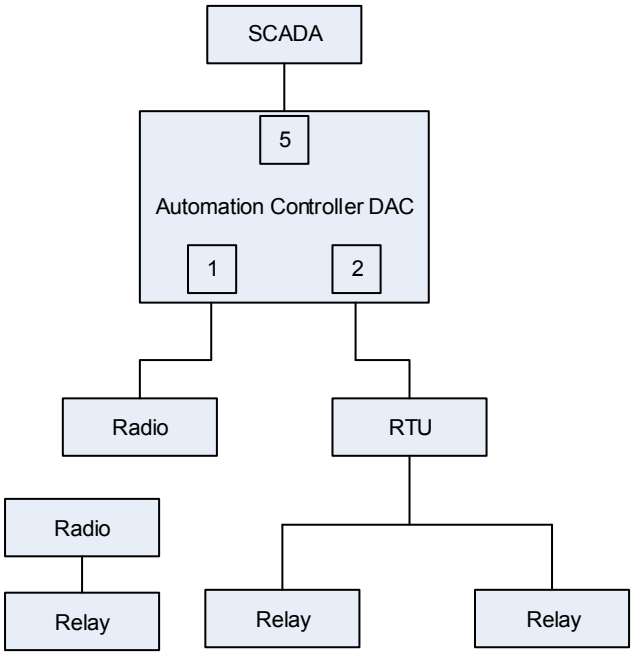


Figure 4.1: Example of ADAC Implementation

4.1.1 Automatic Reconfiguration

The ADAC is capable of automatic reconfiguration (AR) of radial and loop distribution feeders based on the required scheme of operation. A scheme is enabled or disabled by an operator. By default, all feeders are automatically included in a scheme. When a feeder is included in a scheme, it is considered armed. Once the feeder is armed, the ADAC will evaluate the events that may cause AR of this feeder.

The AR system is comprised of three separate sequences: feeder event, feeder return-to-normal, and scheme solution. A brief description of each of these sequences is provided in the following subsections.

4.1.1.1 FEEDER EVENT SEQUENCE

This scheme consists of four sequences: idle, update, analyze, and solution. The purpose of the Idle sequence is to verify whether a feeder is armed. When a feeder is included in a scheme, it is considered armed. When a feeder is not included in a scheme, it is not armed and is in the Idle sequence. The scheme will evaluate events on the feeder. When the feeder is armed and an event occurs on the feeder, the scheme detects this and the sequence transitions to the Update sequence. However, if the feeder is not armed, then the sequence remains in the Idle sequence.

In the Update sequence, an integrity poll of all connected devices is completed to ensure all the subsequent decisions are based on up-to-date information about the distribution network. The integrity poll also helps ensure each device is responsive. If a device is unresponsive, a communications alarm will be generated. The scheme will remain in the Update sequence until all the related devices have responded to the integrity poll. Once this condition is satisfied, the sequence transitions to the Analyze sequence.

The Analyze sequence determines whether a permanent fault, an open-phase condition, or an overload condition exists. This analysis is supervised to ensure the analysis is blocked when an abnormal condition exists in the system. Abnormal conditions are defined to include hot-line tags, nonreclose status, supervisory control disabled, or communications failures. Once the event has been confirmed, the system identifies the feeder sections to consider in the Solution sequence. The DAC will immediately open isolation switches once an event has been confirmed. Confirmed events are reported to the Solution sequence. In the case of a permanent fault, switches are opened to help isolate the fault. The DAC sends the open commands to the isolation switches to allow them to execute while the complete reconfiguration solution is being evaluated. This helps speed up the Reconfiguration sequence.

If the system determines that the event no longer exists, then the sequence returns to the Idle sequence. If the system cannot determine the nature of the event within the time limit for the Analyze sequence, the sequence returns to the Idle sequence. The Analyze sequence default time setting is 120 seconds.

4.1.1.2 FEEDER RETURN-TO-NORMAL SEQUENCE

This scheme consists of four sequences: idle, update, analyze, and reconfigure. The purpose of the Idle sequence is to verify whether a feeder is armed. If the feeder is armed, the sequence remains in the Idle mode until a return-to-normal (RTN) command is detected. The feeder will respond to an RTN command only when the feeder is armed, no abnormal conditions exist on any device in the actual or normal feeder configuration, and there are no supervisory blocks in the program. Once an RTN command is detected, the sequence transitions to the Update sequence.

In the Update sequence, an integrity poll of all connected devices is completed to ensure subsequent decisions are based on up-to-date information about the distribution network. The integrity poll also helps ensure each device is responsive. If a device is unresponsive, a communications alarm will be generated. The DAC will poll all devices in the present feeder configuration, adjacent feeder, all devices in the normal feeder configuration, and all devices in any feeder that is part of the normal configuration of the RTN feeder. The scheme will remain in the Update sequence until all related devices have responded to the integrity poll. Once this condition is satisfied, the sequence transitions to the Analyze sequence.

The Analyze sequence is executed when the system completes the Update sequence. The purpose of the Analyze sequence is to confirm the RTN command should be processed. It verifies there are no abnormal conditions present on any feeders that would be involved in the RTN operations and there are no other events detected in the scheme. Abnormal conditions are defined to include hot-line tags, nonreclose status, supervisory control disabled, or communications failures. If an abnormal condition is detected on a normal feeder configuration, the sequence will abort and return to the Idle sequence. If an RTN command is confirmed, the system identifies all normally-closed (NC) switches on the feeder that are presently open and all normally-open (NO) contacts that are presently closed. These switches make up the minimum set of switches that must be operated to return the feeder to the normal configuration.

4.1.1.3 SCHEME SOLUTION SEQUENCE

This scheme consists of three sequences: idle, analyze, and solution. This sequence is executed in response to confirmed events or confirmed RTN commands reported by the event and RTN sequences described previously.

In the Idle sequence, the system monitors for confirmed events or RTN commands reported by any feeder in the scheme. The system transitions to the Analyze sequence when one or more feeders report a confirmed event or RTN command and all feeders are in the Idle sequence.

The Analyze sequence evaluates scenarios that can be used to address outages caused by permanent faults or open-phase conditions, as well as overload conditions. The system identifies isolation, sectionalizing, and restoring switches for each confirmed event. Isolation switches are identified in the Analyze sequence and reported to the Solution sequence. Once an event has been confirmed, isolation switches must be opened to isolate un-faulted sections of the feeder from the faulted section. All closed switches downstream of a permanent fault, or open phase, are potential sectionalizing switches. Switches with a bypass or inhibit control input asserted are not considered as potential restoration switches. The system identifies all closed switching devices in the affected distribution network that can be used to sectionalize the load. The system also identifies all open switching devices that can be used to restore load. All open switches adjacent to an overloaded feeder are potential restoration switches.

Based on the settings in the DAC system, load transfer operations are selected between feeders that did not experience an event to increase the capacity available to restore stranded load sections. Each scenario is evaluated to determine its validity and relative suitability. Scenarios that involve unavailable sources, or result in permanently connecting multiple sources in parallel, are rejected. If load shedding is disabled, the system rejects all scenarios that result in load shedding.

The scenarios that are not immediately rejected are compared and the best solution is selected. The following criteria (listed in order) are used when evaluating scenarios:

1. Minimize the amount of overload above temporary limits.
2. Minimize the amount of load left de-energized.
3. Minimize the amount of overload above normal limits.
4. Minimize the maximum amount of load allowed to be restored by any one feeder that has voltage above a Level 1 threshold, but below a Level 2 threshold.
5. Minimize the total amount of load selected to be restored by feeders that have voltage above a Level 1 threshold, but below a Level 2 threshold.
6. Minimize switching operations.
7. Minimize the maximum amount of load to be restored by any one non-preferred source.
8. Minimize the total amount of load to be restored by non-preferred sources.
9. Bias the selection toward using the normal source to re-energize load if no overloads above normal limits will result.
10. Maximize the amount of margin below normal limits.

The system favors scenarios with the least number of switching operations. If a solution is found that re-energizes all the affected load and results in all components in the distribution system operating below their normal capacity limits, then the system selects this solution and does not evaluate more complex solutions that require more switching operations. If a complete solution is not found, the system will continue to evaluate more complex scenarios and select the best solution available. The best solution may be a partial restoration or even no action at all. The system will evaluate combinations of up to five sectionalizing switches. In the case of an RTN command, the RTN command sequence identifies the switches to open and close in the Analyze step and reports to the Solution sequence. These switches make up the minimum set of switches that must be operated to return the feeder to its normal configuration; however, other switches may need to be operated to ensure no part of the distribution system is left de-energized because of the RTN operations. If a complete solution cannot be found for an RTN operation, the system will abort and return to the Idle step.

Once the system has found and selected a solution that addresses the events that occurred in the system, the Reconfiguration step is executed. The solution consists of a list of switches to open and close. Isolation switches are identified during the Analyze step of the Event sequence, and these switches will be included in all scenarios evaluated by the DAC. The isolation switches will be opened immediately in the Reconfiguration step. The DAC sends the open command and waits for the status indications from each device to confirm the operations have been completed successfully.

The DAC will restore de-energized zones by closing the selected switch based on a simple set of rules. If the system is using the open-transition switching, the DAC will close the switch if the following conditions exist:

- There is no continuity from the switch to close to the switches to open that are unopened.
- There is only one source connected to one side of the switch to close.
- There is no switching operation in progress on either side of the switch to close.
- There is live voltage on at least one side of the switch to close.

If the system is set to use the closed-transition switching, the DAC will close the switch if the previous conditions exist or if the following conditions exist:

- There are two sources connected, one on each side of the switch to close, that have the same phase relationship and same SourceGroup setting.
- There are no switches to open connected on one side and one or no switches to open on the other side.

- There is no switching operation in progress on either side of the switch to close.
- There is live voltage on at least one side of the switch to close.

Once the solution has been executed, the system transitions to the Idle step. If the system cannot successfully execute the necessary actions, the sequence will fail because it exceeded the ReconfigurationTimeLimit setting. The system will return to the Idle step.

The DAC considers the effect of load when evaluating reconfiguration scenarios. The current flow is measured at various locations throughout the distribution system by IEDs, and this information is communicated to the DAC. The DAC memorizes the calculated load on all components in the distribution network. When an event is confirmed, the DAC will use the memorized load values to determine the suitability of reconfiguration scenarios.

4.1.1.4 PERMANENT FAULT CONDITION

The permanent fault detection is implemented in the "analyze" sequence of the scheme. It is based on fault current indications and lockout indications from switching devices on the feeder. The feeder is evaluated zone by zone, starting at the point farthest away from the source. Fault current indications help identify the switching devices that have experienced fault current. The fault indication farthest from the source will identify the affected zone. Once the faulted zone has been identified, the DAC will wait for a lockout indication before the fault is considered a permanent fault. This is done to allow the local reclosers and breakers to attempt to clear the fault using traditional automatic reclosing methods. If the local automatic reclosing is successful in clearing the fault, the lockout indication will not occur and the fault indications will reset. If the fault is permanent, an upstream breaker or recloser will clear the fault and go to its lockout state. If the coordination of the protection devices is successful, the device closest to the fault will clear the fault and go to lockout. This may not be the case if there is miscoordination of protection devices. In some miscoordination cases, multiple protection devices will go to lockout. To accurately detect this situation, the DAC will force an update poll to all devices on the event feeder when the first lockout indication is detected. Once the DAC has determined that a zone is affected by a permanent fault, the Event sequence will initiate the Solution sequence to find and execute an acceptable solution.

4.1.1.5 OPEN-PHASE CONDITION

Open-phase detection is implemented in the Event sequence. Open-phase detection is based on loss-of-voltage indications from switching devices on the feeder. Before the system detects an open phase, it must first see a healthy voltage level for 30 seconds. This helps to avoid erroneous open-phase detections when lines are first energized. Additionally, voltage indications must show a possible open-phase condition for a period before the Event sequence will initiate. The EventDetectTime setting is assigned during the initial setup of the DAC. The default is 10 seconds, which helps to avoid erroneous open-phase detections during switching operations. The loss of voltage on the feeder could be caused by a fault upstream of the distribution network. The automatic reclosing schemes upstream of the distribution network may be in place to attempt to clear such a fault. Once an open-phase condition has been identified, the distribution network is evaluated to determine if there are any zones downstream of the broken jumper that could be restored by a three-phase source. If an alternative feed is available to energize these zones, the DAC will open the switch downstream of the affected zone to de-energize the downstream zones and prepare them to be restored from the alternative feed. If no alternative feed is available and single-phasing of loads is permissible, the DAC will not open the switch downstream of the affected zone. Instead, the DAC will allow the downstream load to remain energized by one or two phases.

4.1.1.6 OVERLOAD CONDITION

The DAC detects overloads on a feeder if the scheme is enabled, overload detection is enabled, the feeder is armed, no abnormal conditions exist on the feeder, and there is no fault or open-phase conditions on the feeder. Measured currents are filtered by a simple low-pass filter that smooths out step changes and jitters before they are used in the overload detection logic. The overload detection logic uses the maximum of the three filtered phase currents. The logic compares the maximum current to the normal capacity and the temporary capacity limits for the associated equipment. If the maximum current is above the normal capacity, then a Level 1 overload can be detected. If the maximum current is above the temporary capacity, then a Level 2 overload can be detected. Overloads can be detected only on equipment that is neither bypassed nor out of service. The DAC will assert a warning alarm for any

feeder that has a detected overload. This alarm can be passed to a control center to inform an operator of the situation. The Event sequence does not need to be initiated until the confirmation time has nearly expired. The overload is confirmed in the Analyze step of the Event sequence if it is still present after the confirmation time has expired. Once an overload condition has been identified, the distribution network is evaluated to determine if there are alternative feeds available that can be used to alleviate the overload. When a Level 2 overload (i.e., above temporary limits) is confirmed and a load transfer solution is not available, the DAC can perform a load shed to alleviate the overload. The DAC will attempt a load shed only when a Level 2 overload has been present for a period equal to the ShedTime setting.

4.1.2 Dynamic Feeder Optimization

Dynamic feeder optimization (DFO) is the continuous monitoring and discrete control of tap-changing equipment and reactive power sources in the distribution system to improve voltage profiles and power factors in support of power system objectives such as:

- Energy conservation
- Peak power reduction
- Power factor correction or control
- Loss reduction
- Voltage profile optimization
- Reactive power support for transmission

These objectives are interrelated and depend on voltage levels and reactive power flows on the involved feeders.

The DFO system supports the power system objectives by controlling the voltage and reactive power flow on the involved feeders and station bus. The DFO system controls tap-changing devices such as load tap changers (LTCs), feeder regulators, and line regulators. It can also control reactive power sources, which can include bus capacitor banks and line capacitor banks. The capacitor control provides coarse voltage control and power factor control while the regulator tap control provides fine voltage control.

4.1.2.1 DISTRIBUTION UNIT CONTROL

A distribution unit is a collection of a station transformer, a station bus, and the connected feeders. The DFO system provides integrated critical limits, control functions, and optimization at all three levels of the distribution unit.

The critical limits define a range of acceptable voltage and power factors, and the DFO system acts to correct any excursions beyond these critical limits. The control functions include user-defined set points and dead-band values, which define a narrow range of desired voltage, power factor, and reactive power. The DFO system acts to correct excursions beyond these control limits. Optimization functions work to gain improvements in the overall performance of the distribution unit. The priority of each function varies. The critical limits are processed with a higher priority than control functions, and control functions are processed with a higher priority than optimization functions.

The DFO system provides reactive power control or power factor control at the high side of the station transformer. When the reactive power control is enabled, the DFO system acts to control the reactive power to a user-specified reactive power set point within a reactive power dead band. When power factor control is enabled, the DFO system acts to control the power factor to a user-specified power factor set point within a reactive power dead band.

The DFO system provides critical voltage limits and power factor limits, as well as power factor control at the station bus. When any control functions in the distribution unit are enabled, the DFO system acts to drive the bus voltage and power factor within user-specified high and low limits. The DFO system also avoids operations that are predicted to drive the bus voltage or power factor outside of the high or low limits. The critical limits at the station bus have a higher priority than control and optimization functions at all levels of the distribution unit. When the power factor control is enabled on the bus, the DFO system acts to control the power factor to a user-specified power factor set point within a reactive power dead band.

The DFO system provides voltage limits and power factor limits, as well as power factor control and minimum voltage control for each feeder. When the feeder functions are enabled, the DFO system acts to drive all measured voltages on the feeder within user-specified high- and low-voltage limits. Additionally, the DFO system acts to drive the power factor at the head of the feeder within high- and low-power factor limits. The DFO system also avoids operations that are predicted to drive voltage or power factor outside of the high or low limits. The DFO system acts to optimize voltage profile and reactive power flow on the feeder.

In some cases, the critical limits and the control and optimization objectives are interrelated and can be in opposition. Therefore, the objectives are prioritized to resolve any potential conflicts. The following list presents the priority of the objectives, starting with the highest priority:

1. Critical voltage limits on feeders
2. Critical power factor limits on feeders
3. Critical voltage limits on bus
4. Critical power factor limits on bus
5. Minimum voltage set point on feeders
6. Power factor or reactive power control at station transformer high side
7. Power factor control bus
8. Voltage and reactive power optimization on feeders

4.1.2.2 DFO SEQUENCE OF OPERATION

The DFO sequence of operation consists of five steps: ready, plan, select, execute, and verify.

In the ready step, the system monitors for DFO requests. A DFO request can be initiated by a critical excursion, control excursion, mode change, set-point change, preconfigured cyclic interval, or a re-evaluation request generated in the Verify step. When the DFO is enabled, a control excursion generates a DFO request when a control limit is violated in the distribution unit. A mode change at any level in the distribution unit will generate a DFO request. A change in the set point for any enabled control function in the distribution unit also generates a DFO request.

In the plan step, the system evaluates a series of possible control scenarios. Each scenario can have multiple control actions. Only the control actions that are presently available to the DFO system are considered. The maximum number of control actions to consider in a scenario is specified by the user. The voltage and reactive power impact of each scenario is predicted, and scenarios are evaluated based on the priorities of objectives previously listed. The plan may be to do nothing, do one control action, or do multiple control actions. If the plan is to do nothing, then the sequence returns to the ready step. Otherwise, the sequence progresses to the select step.

In the select step, the system evaluates each control action in the plan to determine which control action to execute first. If the plan includes control actions, then the Select step will identify one control action in the plan. The voltage and reactive power impact of each control action in the plan is predicted, and each control action is evaluated based on the priorities of objectives previously listed. Once a control action is selected, the sequence progresses to the Execute step.

In the execute step, the DFO system issues controls and monitors device feedback and system response to perform and validate the selected control action. Once the control action is executed, the sequence progresses to the Verify step.

In the verify step, the DFO system evaluates the distribution unit to determine the effectiveness of the preceding control action. Once the verification is complete, the sequence returns to the Ready step and asserts a DFO request to re-evaluate the distribution unit to update the plan for possible subsequent control actions.

4.1.2.3 AVAILABILITY OF CONTROL ACTIONS

Several conditions affect the availability of a control action to the DFO system:

- If the DFO functions on a feeder are disabled, all devices on the feeder are unavailable.
- If the DFO functions on a device are disabled, the device is unavailable.
- If control of a device is inhibited, the device is unavailable.
- If a communications failure is detected for a device, all control actions associated with the device are unavailable.
- If a capacitor has been switched an excessive number of times in the same day, the capacitor is marked unavailable for the remainder of the day (until midnight).
- If the last attempted operation of a capacitor was bad, the capacitor is marked unavailable for a user-specified period or until the capacitor function block receives a Reset command.
- If the last attempted operation of a regulator was unsuccessful, the associated set of three regulators is marked unavailable for a user-specified period or until the regulator function block receives a Reset command.
- If a regulator is at the high tap limit, additional "raise" tap operations are unavailable. Similarly, if a regulator is at the low tap limit, additional "lower" tap operations are unavailable.

4.1.2.4 REGULATOR RESPONSE

When the DFO system operates a regulator, the system monitors the regulator tap position and the regulated voltage to verify the response to the control action. The success of the operation is determined by the response of the regulated voltage. If the regulated voltage is greater than a user-defined percentage of the expected response, the operation is successful. If the regulated voltage does not reach the expected response within the user-defined response time, the operation is not successful and a warning alarm is issued. If the last three attempted operations of a regulator are unsuccessful, a failure alarm is asserted and the associated set of three regulators is marked unavailable for a user-specified period. When this time expires, the failure alarm will clear and the regulator will become available to the DFO system.

4.1.2.5 CAPACITOR RESPONSE

When the DFO system operates a capacitor, the system monitors the capacitor switch status and the feeder VAR response to verify the response to the control action. A feedback trouble alarm is generated if the expected switch status is not received within a user-specified response time. This alarm is only a warning and does not determine the success of the operation. Two user-specified percentages and a user-specified response time are used to determine the success of the operation. One user-specified percentage defines the percent of the expected VAR response, above which is considered a good response. The other percentage defines the percent of expected VAR response, below which is considered a bad response. If the capacitor has three consecutive partial operations, the operation is also considered to be a bad operation. If the last attempted operation of a capacitor was bad, then a failure alarm is asserted and the capacitor is marked unavailable for a user-specified period. Once this period expires, the failure alarm will clear and the capacitor will become available to the DFO system.

4.1.2.6 DFO AND DEVICE CONTROL MODES

The DFO system is an automatic system that issues remote control operations to end devices. Many of the end devices that participate in the DFO system also have local automatic control capabilities. When the DFO functions on a feeder are disabled, the DFO system sends a command to the end device informing it that the remote automatic system is no longer controlling the end device. The local device control can use this indication to enable local automatic control functions. The DFO system can be configured to send a periodic Watchdog command to the end devices. This Watchdog pulse can be monitored by the end device controller. If the pulse is not received for an extended period, the local device control can be set to enable local automatic control functions. Typically, device controllers will have a Remote or Local mode and an Automatic or Manual mode. In the Remote mode, the controller accepts commands from remote systems, such as a SCADA master or the DFO system. In the Local mode, the controller will not accept commands from these remote systems.

4.1.2.7 CAPACITOR CALIBRATION

The expected voltage change on a feeder in response to a capacitor switching depends on the size of the capacitor and its location on the feeder. The size of the capacitor is specified by the user; however, the location of the capacitor is not. The user provides only the relative positions of equipment on the feeder. The expected voltage response at a point on the feeder is dependent on the impedance between that point and the source. The DFO system does not require the user to provide detailed impedance data during system setup. Instead, a calibration procedure is used to estimate the reactance between each voltage measurement point on the feeder to the source.

The following calibration procedures should be performed when the feeder load is stable:

Step 1. User opens capacitor switch.

Step 2. User disables the DFO system.

Step 3. User resets the capacitor warning and failure alarms.

Step 4. User asserts the calibrate input on the capacitor function block.

Step 5. DFO system closes the capacitor switch.

Step 6. DFO system monitors the power system response.

Step 7. DFO system opens the capacitor switch.

If the capacitor operation is not successful, the DFO system asserts the capacitor fail alarm.

If the capacitor operation is successful, the DFO system asserts the capacitor calibration completed indication.

The calibrate input on the capacitor function block is deasserted by the user.

4.2 PMU-ENABLED SOLUTIONS

PMUs have been used in numerous applications such as testing, commissioning, disturbance recording, and wide-area protection and control to improve power system operations. With PMUs available in protective relays, meters and recorders, it has become easier to implement synchrophasors in diverse applications.

PMUs provide a way to analyze both small and large disturbances in a power system. PMUs provide the following three basic elements unlike the traditional measurement methods:

- Data stream rates of 1 to 60 messages per second.
- Synchronized measurements from all locations using high-accuracy timing.
- High-accuracy measurements of voltage, current, status, and alarms.

Applications for PMUs are listed in the following subsections.

4.2.1 Islanding Detection

Islanding is a condition in which a distributed generator continues to power a location even though electrical grid power from the electric utility is no longer present. The expansion of generation into the distribution system has had a specific impact on the ability to detect islanding in a portion of the system. If a section of the distribution system is supported by a single feeder with a single circuit breaker, it is a simple process to detect when the breaker is opened and then it signals the generator to disconnect from the system. However, this is not always the case. Consider a distribution network that is configured with both radial and loop systems and interconnected with multiple breakers to provide reliable service to critical loads. In such a case, it would be difficult to determine which combination of open breakers and switchgear would cause a generator on the distribution network to be islanded with nearby connected loads.

Unintentional islanding is not a desirable operating condition. If power lines remain energized when the utility interconnection is lost, this poses a risk to utility workers in the field. Islanding also causes voltage and frequency to fall outside acceptable levels, which results in power quality issues.

Wide-area communications, combined with PMU capability in relays, make it possible to detect islanding at any location (that uses distributed generation) for no extra cost. IEEE 1547 requires distributed generation to disconnect for an islanding condition in 2 seconds or less, regardless of the load generation balance. Traditional islanding detection schemes use frequency and voltage measurements at the generator. A modern system based on PMU measurements at both the generator and remote station provides better sensitivity and speed to meet the requirements of IEEE 1547. PMUs can also help by improving generator control during islanding when the generator control is required to switch from power regulating to frequency regulating before the machine goes unstable.

4.2.2 Phase Identification

Improper phase identification causes problems with load balance, fault location and targeting, metering, and other reliability issues. With service quality becoming more important to engineer and public service commissions, phase identification has become even more significant. As computerized fault location becomes more practical, and with increased inputs from multiple IEDs, it becomes both important and perhaps easier to provide phase identification. Because of the increased availability of microprocessor-based smart controls and communications, more single-phase control and monitoring are being used. Moreover, modern recloser controls offer adaptive multiphase or single-phase tripping. Proper phase commissioning is essential for correct operation of these reclosers. Correct phase identification is also important for applications involving microprocessor-based regulators and capacitor bank controls to ensure the volt/VAR optimization scheme is operating with the correct data.

With distributed IEDs, the opportunity exists to apply distributed PMUs for phase identification. Using a synchrophasor enabled meter, it is simple to either manually or automatically identify phases.

4.2.3 Load Characterization

PMUs help provide a better understanding of distribution loads and how they are impacted by changing grid conditions. PMUs can collect data from voltage regulator controls that provide timed events with power, voltage, current, frequency, and changes in power and reactive power voltage steps. Collecting these data for individual feeders will help identify potential feeders where conservation voltage reduction (CVR) can be implemented. CVR is a technique for improving the efficiency of the electrical grid by optimizing voltage of the feeder lines that run from the substation to the customer. CVR lowers the voltage at which power is delivered and yields, on average, a 1 percent energy savings for each 1 percent in voltage reduction. The high-resolution data collected by PMUs from the regulator control can help calculate the change in power that occurs coincident with the tap changes. With multiple PMUs providing information from different feeders, the additional information will help improve the load characterization of the system to assess the impact of CVR. In this way, PMUs can help in determining necessary actions for maintaining reliability of the distribution system when there are varying loads.

4.2.4 System Monitoring

PMUs strategically placed at locations in the secondary system can help provide more insight about the system and enable detection of system conditions and local voltage transients. PMUs connected to the distribution system can detect system phase shifts, frequency, and oscillations. PMUs connected closer to the load in a distribution system can provide a better understanding of the dynamics of the connected load.

4.3 HIGH-IMPEDANCE FAULT DETECTION

High-impedance faults (HIFs) are short-circuit faults with fault currents smaller than what a traditional overcurrent protective relay can detect. Common causes for an HIF are tree branches touching a phase conductor, failing or dirty insulators that cause flashovers between a phase conductor and the ground, or a downed conductor. Almost all HIFs involve the ground directly or indirectly.

HIFs are rich in harmonic and nonharmonic content. The harmonic content results from a fault that involves an arcing process. Ungrounded systems have no intentional grounding. The ground-fault current is determined by fault resistance and stray capacitances of distribution transformers. These systems offer minimum equipment thermal stress and self-extinction of ground faults when the capacitive fault current is small. However, in a large grounded system (solidly grounded or low-impedance grounded), the fault is less likely to self-extinguish because the stray capacitance can support enough fault current. Solidly grounded systems limit the risk of overvoltages during ground faults and reduce equipment cost; however, these large current grounding schemes produce large standing unbalance that flows in the same path as the ground-fault current. This makes it difficult to detect HIFs.

Staged downed conductor tests have indicated that downed conductor HIFs generate small fault currents. The HIF current of multigrounded systems depends on the surface types upon which a conductor falls. Fault current varies from 0 to less than 100 A. These faults are masked by load unbalances in solidly grounded distribution systems. Traditional ground overcurrent elements cannot detect these faults. Detection algorithms that use current characteristics other than magnitude must be used for this purpose.

The block diagram of the HIF detection method is shown in Figure 4.2.

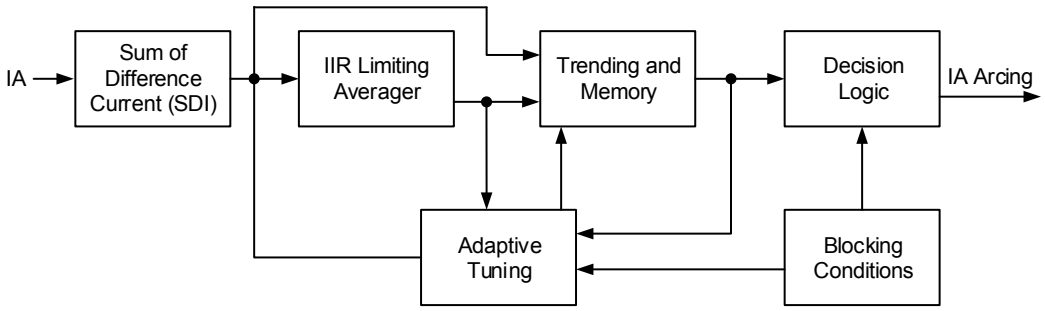


Figure 4.2: Block Diagram of HIF Detection (Nonharmonic)

The HIF detection method incorporates the following key elements:

- A quantity that reveals the HIF signatures without being affected by loads and other system operation conditions.
- A running average of the quantity that provides a stable prefault reference.
- An adaptive tuning feature that can tune out feeder ambient noise conditions.
- Logic to differentiate between an HIF condition and other system conditions such as switching operations and noisy loads.

The first function block calculates a signal quantity upon which the algorithm bases its HIF detection. This quantity is called the sum of difference current (SDI). The Infinite Impulse Response (IIR) limiting averager then establishes

a stable reference for the SDI. The trending and memory block compares the present SDI to the SDI average. It memorizes the time and ratio of the present SDI if the present SDI is greater than a set threshold for the SDI average. The decision logic uses the results from the trending and memory block to determine the existence of an HIF on the processed phase. The adaptive tuning block monitors feeder background noise during normal operating conditions and establishes a comparison threshold for the trending and memory block. This threshold is also used by the IIR limiting averager to prevent the averager input magnitude from becoming too large.

HIF detection depends on the system grounding scheme. For small-current grounding, fault detection is relatively easier because the standing unbalance comes only from line construction asymmetry and phase CT errors. However, this unbalance is normally small and modern microprocessor relays can be sensitive enough to detect most HIFs. For large current grounded systems, the detection of HIFs is more challenging because there is high standing unbalance because of single loads. Because the HIF current is less than the standing unbalance, quantities other than the fundamental value or rms value of current will be used for detection purposes. Harmonic content is usually used for HIF detection.

HIF detection technology is available in relays supported by Vendor L. As previously mentioned, these devices use both nonharmonic and odd-harmonic content for HIF detection.

4.4 FAULT LOCATION

The ability to locate and clear line faults is imperative to reduce the frequency and duration of power outages. Utilities often use the short-circuit analysis results of their distribution feeder and the measured fault current to identify possible fault locations in a feeder. This method provides good results if the fault resistance is negligible and the short-circuit analysis uses the actual system voltage during the fault.

Vendor L supports digital relays with built-in fault location capabilities. These relays accurately locate all fault types by measuring and using the phase-to-ground voltages and currents in each phase. The phasor quantities are filtered to ensure that transients do not affect the measurements. These measurements are used for determining the fault type. Knowledge of the fault type is important for accurate single-end fault locating.

The relays use the measured voltage and current in each phase to calculate the impedance. The distance to the fault is then determined using the details of the line programmed in the relay.

Fault location on distribution feeders is difficult. Traditional impedance-based fault location methods assume all feeder sections have the same impedance characteristics. However, this is not usually the case with distribution feeders that may contain sections with different conductor types and different tower configurations.

Protective relay supported by Vendor L provide differential protection and distance protection, and include the traveling-wave fault location (TWFL) feature. This relay is mainly used for transmission line applications. However, it addresses some of the challenges faced by fault location applications on distribution feeders.

The relay monitors the protected line. When a fault occurs on the line, the transient generated by the fault moves toward the relay location. The TWFL algorithm relies on the transient wave received by the relay. Once the transient is received by the relay, it is time-stamped using a high-accuracy IRIG-B signal and the information regarding the time stamp is communicated to the relay at the far terminal using a differential communications channel. Using the length of the line, the propagation velocity, and the secondary cable length of the CT, the relay can calculate the location of the fault.

The relay uses several methods for determining fault location, including:

- Traveling wave (TW)
- Multiended (ME)
- Single ended (SE)

As previously mentioned, the TWFL algorithm uses the differential communications channel to communicate information to the relay at the far terminal. For this method to be successful, a healthy differential communications channel is required.

The double-ended fault location is an impedance-based method that is used when a differential communications channel is present. Information regarding the total current is available to relays at each location and this quantity is used as a polarizing quantity to achieve results that are more accurate than the single-ended method.

The fault location method does not make use of the differential communications channel. This is an impedance-based method that uses a modified Takagi algorithm to calculate the distance to the fault using the voltage and current at the relay location.

The presence of different tower configurations, different conductor size and spacing, conductor transposition, and series capacitance should not prevent the use of traveling waves for fault location. However, the variation in electrical characteristics across the protected line could impact the propagation velocity and could lead to an error of 1 to 2 percent in the fault location distance estimation. This opens the possibility to use TWFL for fault location on distribution feeders; however, further testing is required before this option can be implemented.

4.5 DYNAMIC LINE RATING IN DISTRIBUTION CIRCUITS

Typically, the ampacity of distribution lines is set at conservative values for various seasons based on a set of assumptions such as ambient temperature, wind speed, and solar heating input. These conservative thresholds often limit the operation efficiency of the grid.

Dynamic rating is the ability to calculate the distribution line ratings based on environmental conditions. The ampacity of a conductor, in addition to the conductor type and material, heavily depends on the temperature of the conductor. One way to implement dynamic rating is to use line thermal protection.

Line thermal protection consists of monitoring the conductor temperature and generating a trip signal when the temperature becomes greater than the maximum allowed temperature for the conductor. Lines that are thermally overloaded will develop excessive sags. This can, in turn, increase the risks of faults from contact with nearby objects.

Line thermal protection is implemented by using control equations to emulate first-order heat-balance equations. The heat input to a conductor is based mainly on the heat dissipated in the conductor because of resistance, solar heat gain, and ambient temperature. Heat losses are mainly because of convection and radiation losses. An illustration of this is shown in Figure 4.3. These principles and procedures have been standardized in IEEE 738-1993, IEEE Standard for Calculating the Current-Temperature of Bare Overhead Conductors.

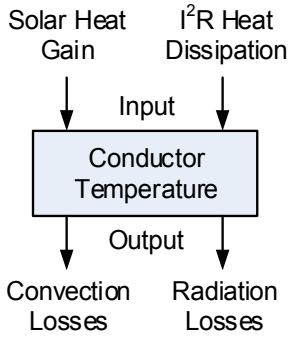


Figure 4.3: Balance Equation Schematic

The equations relate the difference between heat input and output to the heat thermal capacity of the conductor. The heat power input is calculated using the position of the conductor, day of the year, and time of the day. The protection provides an option for RTD measurements for ambient temperature. Once the equations have been programmed into the relay, the protection logic is run iteratively to calculate the conductor temperature. The logic can be programmed to alarm at a low temperature threshold and trip at a high temperature.

Research shows that line thermal protection schemes have been successfully implemented for transmission lines using Vendor L relays. However, differences in conductor types and different tower configurations may cause errors

in the thermal equation calculations. Before implementing this scheme to distribution circuits, through testing should be carried out.

4.6 BASELINE DATA

Baseline data was collected to understand the existing system characteristics for the selected distribution circuits. This data was used as reference for analysis during RTDS test runs.

1. The following list of attributes was prepared as reference for collecting baseline data. Field data was collected depending on its availability:

    a. Voltage profile

    b. Frequency

    c. Harmonics

    d. Power factor

    e. Load profile

2. Appendix B Load Profile includes the load profile data acquired over a period of 24 hours for the three selected circuits.

3. The following standards for voltage, frequency, harmonics distortion limits, and power quality indices were referred to for analysis:

    a. ANSI C84.1-2006 American National Standard for Electric Power Systems and Equipment – Voltage Ratings (60 Hertz).

    b. IEEE 1366-2012, IEEE Guide for Electric Power Distribution Reliability Indices.

    c. IEEE 1159-2009, IEEE Recommended Practice for Monitoring Electric Power Quality.

    d. IEEE 1547-2003, IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems.

5 RTDS MODELING

This section describes the process involved in the test circuit data collection and conversion into RSCAD which is used for analysis and testing. It also describes the modelling assumptions made during conversion. The process followed for modelling of the RTDS load control, based on the load data available for the selected test circuits is described.

5.1 SYNERGI TO RTDS CONVERSION PROCESS

Three diverse types of distribution circuits were considered for this project, namely coastal-residential, urban, and desert-rural. The circuits were originally in the Synergi Electric software format. The original circuits were analyzed and simplified based on the requirements and scope of this project. The following assumptions or simplifications were made:

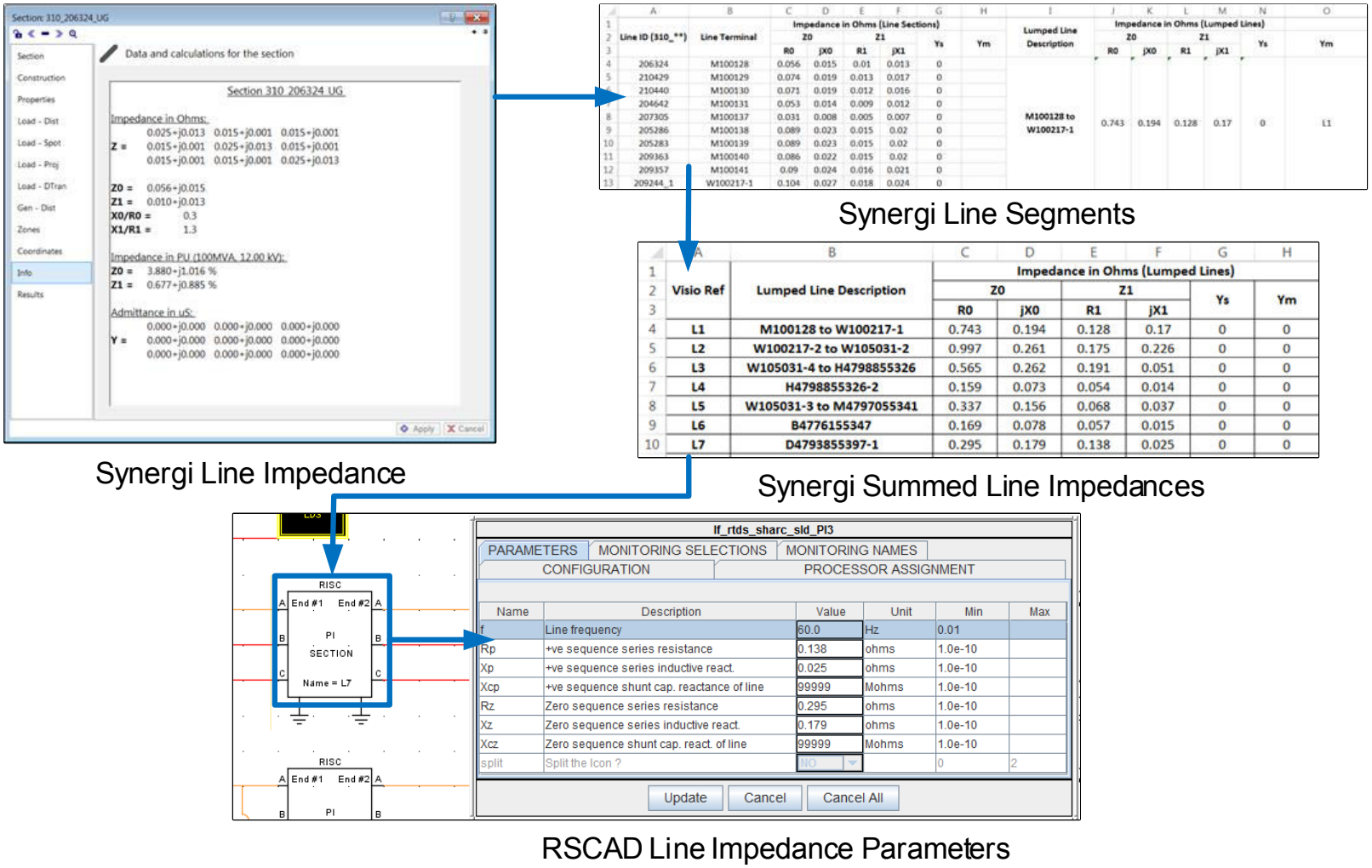
- The Synergi Electric model was converted into a 12 kV equivalent model, with the single and three phase loads and line impedances lumped.
- Fuses and switches were ignored in the 12 kV equivalent.
- The DER source was modeled as a scalable battery system.
- Harmonic sources or loads were disregarded in the 12 kV equivalent.

The simplified circuit one line were drafted using a visualization software and further translated to RSCAD, version 5.001. Refer to Appendix A for more details on the simplified circuit one line drawings. Each circuit was modeled on a single RTDS rack with a time step of less than 150 milliseconds. Field load profile data were provided by SDG&E for each circuit. The RTDS model was validated based on the field data and compared to the Synergi model for accuracy. This section explains the conversion of the Synergi data to RSCAD.

5.1.1 Line Impedance Conversion – Synergi to RSCAD

The Synergi model distribution lines were divided into multiple sections. Each section contained its own identifier and set of impedances that are represented in the upper left of Figure 5.1. The line identifier and impedances are recorded in a spreadsheet in the upper right of Figure 5.1. The distribution line segments from one intersection to the next are given a name using their respective terminal identifier from Synergi model. The impedances are summed together in Figure 5.1 (labeled “Synergi Summed Line Impedances” in the center of the figure) and given a new name (L1, L2, L3, etc.). L1 starts from the substation and turns into L2, L3, and so on, down the distribution lines. The lumped line impedances are entered in the RSCAD transmission line impedance block (PI section), as shown in the lower section of Figure 5.1. This is the last step in translating the line impedances from the Synergi model to RSCAD.

5.1.1.1 LINE IMPEDANCE CONVERSION



Line ID (310_**)	Line Terminal	Z0 R0	Z0 jX0	Z1 R1	Z1 jX1	Ys	Ym	Lumped Line Description	Lumped Z0 R0	Lumped Z0 jX0	Lumped Z1 R1	Lumped Z1 jX1	Lumped Ys	Lumped Ym
206324	M100128	0.056	0.015	0.01	0.013	0								
210429	M100129	0.074	0.019	0.013	0.017	0								
210440	M100130	0.071	0.019	0.012	0.016	0								
204642	M100131	0.053	0.014	0.009	0.012	0								
207305	M100137	0.031	0.008	0.005	0.007	0		M100128 to W100217-1	0.743	0.194	0.128	0.17	0	L1
205286	M100138	0.089	0.023	0.015	0.02	0								
205283	M100139	0.089	0.023	0.015	0.02	0								
209363	M100140	0.086	0.022	0.015	0.02	0								
209357	M100141	0.09	0.024	0.016	0.021	0								
209244_1	W100217-1	0.104	0.027	0.018	0.024	0								

Visio Ref	Lumped Line Description	Z0 R0	Z0 jX0	Z1 R1	Z1 jX1	Ys	Ym
L1	M100128 to W100217-1	0.743	0.194	0.128	0.17	0	0
L2	W100217-2 to W105031-2	0.997	0.261	0.175	0.226	0	0
L3	W105031-4 to H4798855326	0.565	0.262	0.191	0.051	0	0
L4	H4798855326-2	0.159	0.073	0.054	0.014	0	0
L5	W105031-3 to M4797055341	0.337	0.156	0.068	0.037	0	0
L6	B4776155347	0.169	0.078	0.057	0.015	0	0
L7	D4793855397-1	0.295	0.179	0.138	0.025	0	0

Name	Description	Value	Unit	Min	Max
f	Line frequency	60.0	Hz	0.01	
Rp	+ve sequence series resistance	0.138	ohms	1.0e-10	
Xp	+ve sequence series inductive react.	0.025	ohms	1.0e-10	
Xcp	+ve sequence shunt cap. reactance of line	99999	Mohms	1.0e-10	
Rz	Zero sequence series resistance	0.295	ohms	1.0e-10	
Xz	Zero sequence series inductive react.	0.179	ohms	1.0e-10	
Xcz	Zero sequence shunt cap. react. of line	99999	Mohms	1.0e-10	
split	Split the Icon ?	NO		0	2

Figure 5.1: Line Impedance Conversion From Synergi to RSCAD

5.1.2 Load Impedance Conversion – Synergi to RSCAD

Single-phase and three-phase loads are represented in Synergi for the test circuits. To model these loads in RSCAD, a similar process as that of the distribution line impedances was followed. The Synergi load distribution settings (upper left of Figure 5.2) were taken and recorded into a spreadsheet (upper right of Figure 5.2). This was done to each load in the system. The recorded loads were given an identifier using the designated name from Synergi and are shown in the upper right of Figure 5.2. Recorded with each load identifier are the real and reactive power values. Loads were then summed to an equivalent impedance per bus to reduce the circuit and simplify the representation that is labeled "Summed Load Data" in Figure 5.2. These data were entered in the RSCAD dynamic load block (lower part of Figure 5.2) for RTDS testing.

5.1.2.1 LOAD IMPEDANCE CONVERSION

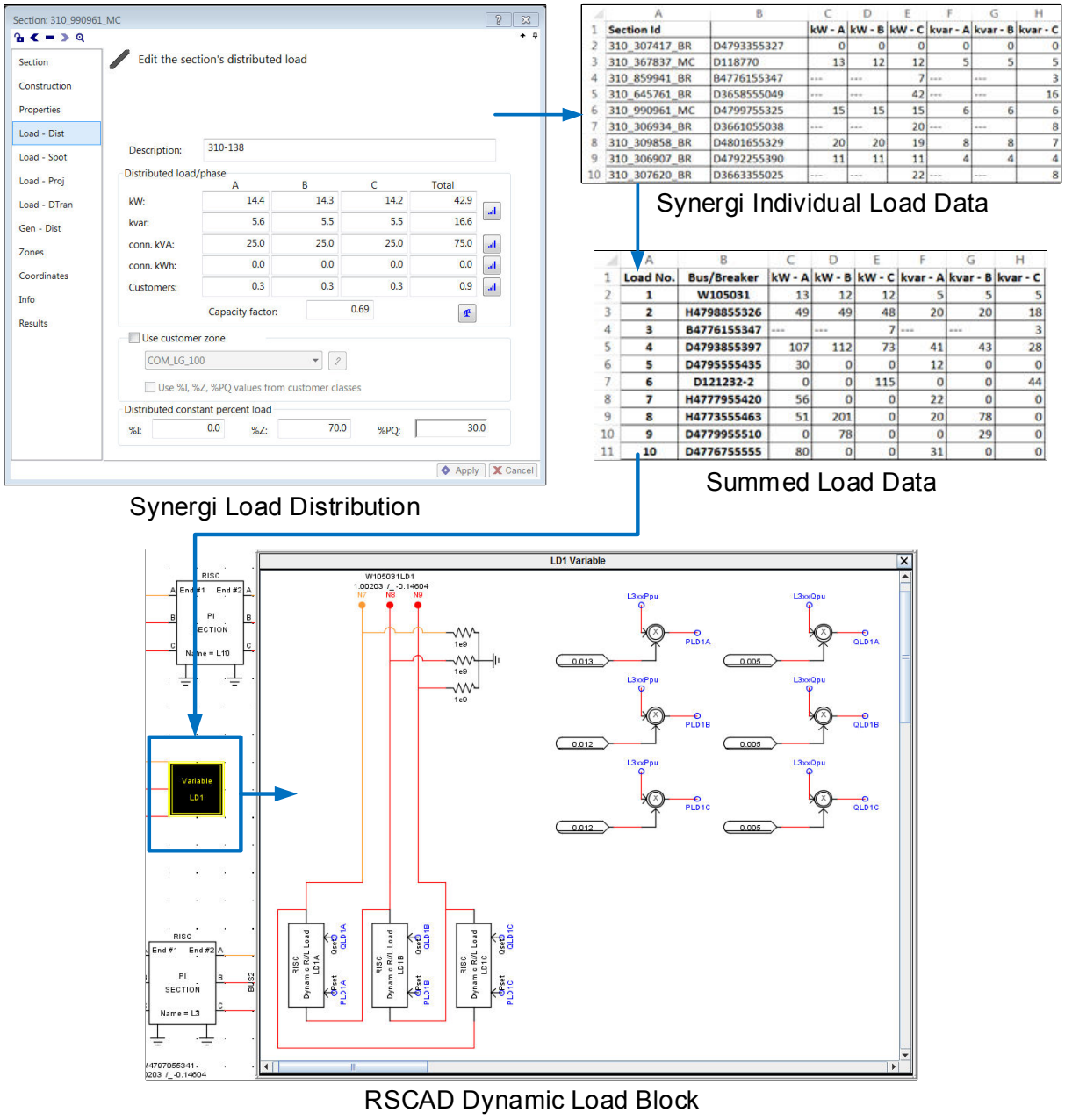


Figure 5.2: Load Impedance Conversion From Synergi to RSCAD

5.2 RTDS CONTROLLER

5.2.1 RTDS Load Impedance Controller

The RTDS can vary the load dynamically via the RunTime view or by running automated load schedulers. SDG&E provided a 24-hour load profile for the three test circuits, namely coastal-residential, urban, and desert-rural. Figure 5.3 shows the load profile of the coastal-residential test circuit. The 24-hour field profile was condensed to a 1-hour segment for lab testing. These data were recorded in a spreadsheet and then converted into a format that is compatible with RSCAD to create an automated load scheduler. Figure 5.4 shows the RSCAD load control input that can be controlled via the RunTime interface or the automated load scheduler. This selection is made via the toggle switch, LPSELECT. The RunTime interface in Figure 5.5 contains slider controls to manipulate the real and reactive power of the loads as a percentage of their maximum capacity.

5.2.1.1 LOAD IMPEDANCE PROFILE AND CONTROL

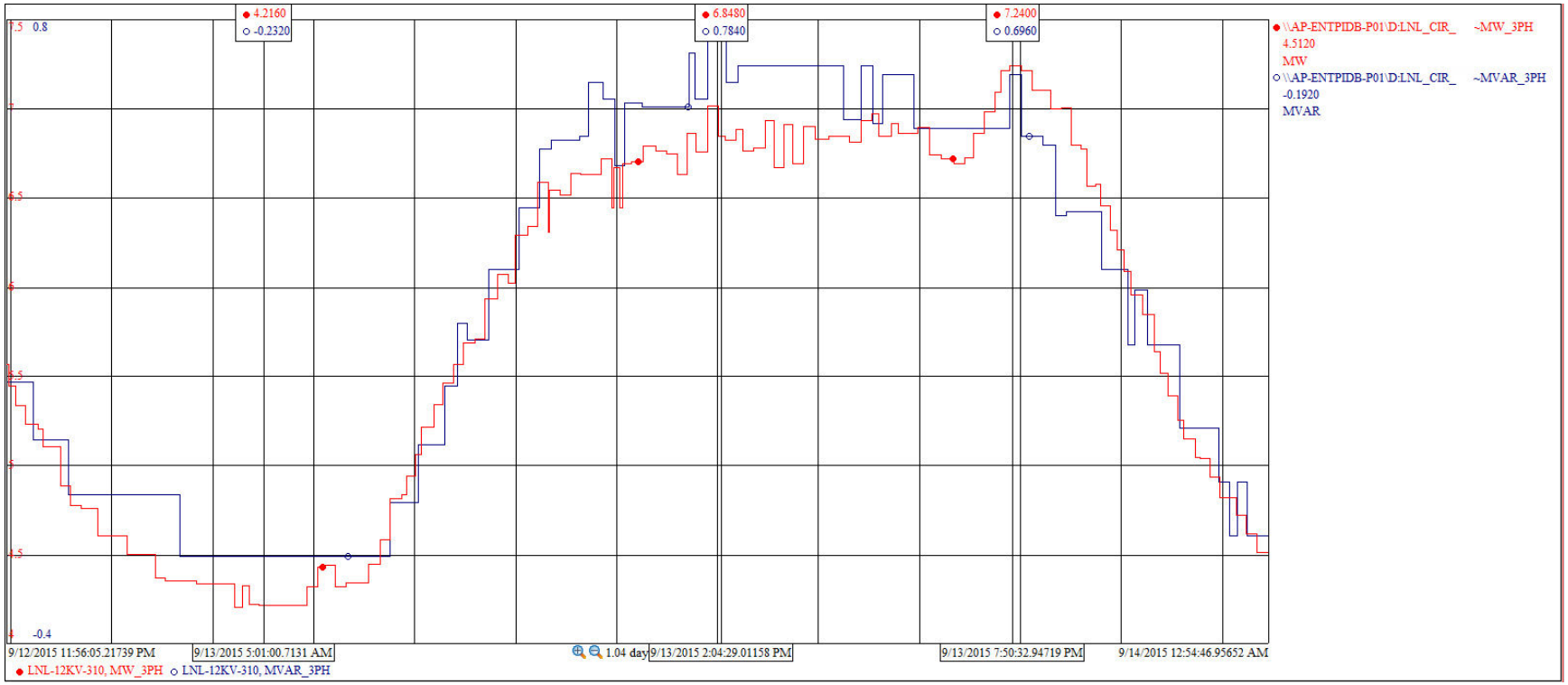


Figure 5.3: Coastal-Residential Test Circuit – 24-Hour Field Load Profile

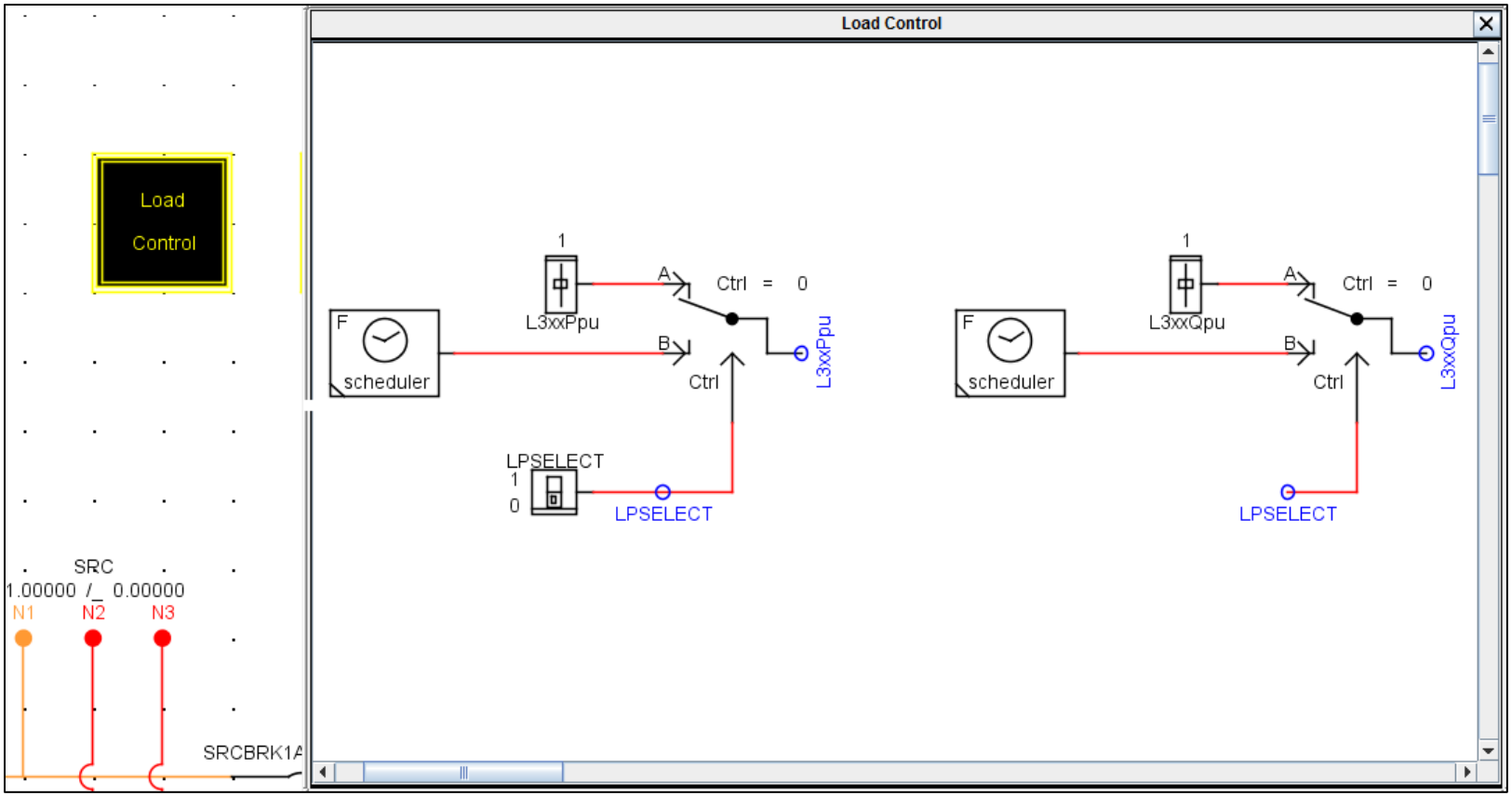


Figure 5.4: RSCAD Load Control

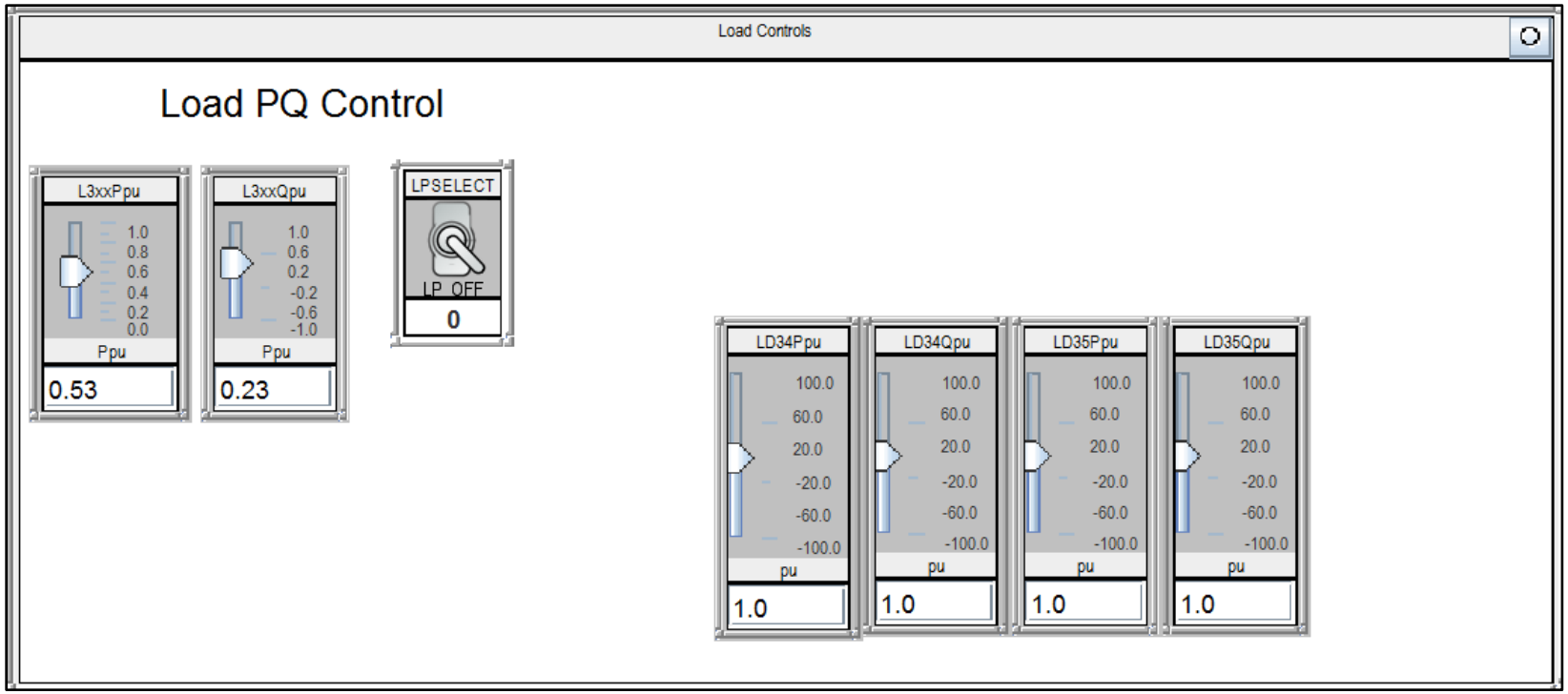


Figure 5.5: RSCAD Load Control HMI

5.3 RESULTS CAPTURE

A visualization and analysis software was used for capturing results and alarms for all test cases in this project. Phasor, analog, and digital data tags are sent from the relay under test to a data concentrator over IEEE C37.118 protocol. The data concentrator sends these tags to the visualization software where these tags are analyzed and arranged into their respective device graphs. The test results in real time are available to the user for various test scenarios. These graphs can be used for continued analysis of each test case.

RSCAD RunTime was also used to capture test results.

6 VOLTAGE REGULATOR CONTROL TESTS

This section provides the test procedure to study the existing SDG&E voltage regulator controls. The purpose of this study is to analyze the capabilities and controls of a voltage regulator as a stand-alone voltage support device in a distribution circuit. These tests would provide useful data for the development and implementation of voltage coordination scheme using multiple voltage support devices. The results from this study will also provide suggestions for improvements for optimal performance of the voltage regulators. The voltage regulator used in these tests works with a tap-changing automatic transformer to regulate distribution line voltages.

6.1 TEST SETUP

The hardware setup of the test circuit is shown in Figure 6.1. The circuit involving the voltage regulators is simulated on the RTDS and the load-side and source-side voltages are derived from the circuit. These voltages, as the low-level signals, are amplified using Vendor B amplifier and fed to the voltage regulator control. This study uses three voltage regulator controls, one for each phase.

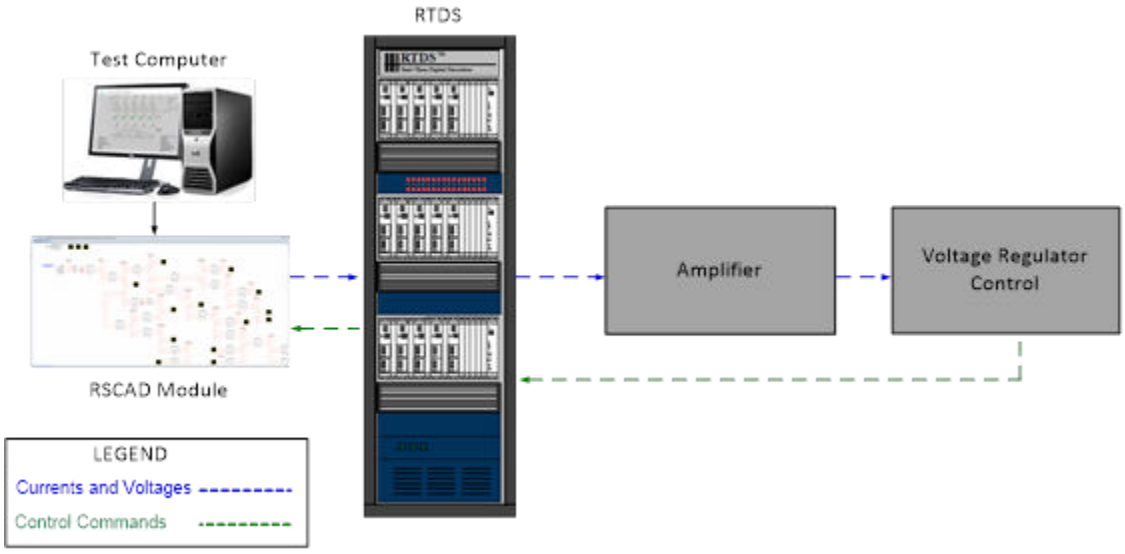


Figure 6.1: Voltage Regulator Control Test Setup

6.1.1 Voltage Regulator Control LED Definitions

The voltage regulator operation and indication light-emitting diodes (LEDs) are located on the front panel of the control. Table 6.1 lists the details for each LED. The device has 11 programmable LEDs and 11 operator-controlled pushbuttons.

Table 6.1: Voltage Regulator Operation and Indication LED Definitions

LED Name	Color	Description
NEUTRAL POSITION	Yellow	Voltage regulator is in the neutral position.
ENABLED	Green	Voltage regulator control is enabled.
ALARM	Red	Follows the state of the programmable setting ALARM.
VOLTAGE REDUCTION	Yellow	Voltage reduction in progress.
AUTO INHIBIT	Yellow	Illuminates when automatic tap changers are inhibited.
REVERSE POWER	Yellow	Reverse system power flow detected.

LED Name	Color	Description
VOLTAGE HIGH LIMIT	Red	When illuminated, the system load-side terminal voltage exceeds voltage limit setting VMAX.
HIGH BAND	Yellow	Regulated voltage is above the high-band threshold.
IN BAND	Green	Regulated voltage is between the high-band threshold and the low-band threshold.
LOW BAND	Yellow	Regulated voltage is below the low-band threshold.
VOLTAGE LOW LIMIT	Red	When illuminated, the system load-side terminal voltage is below the voltage limit setting.

6.1.2 Voltage Regulator Operator-Controlled Pushbuttons

Table 6.2 lists the possible functions of the operator-controlled pushbuttons. These pushbuttons display the desired information on the device LED screen.

Table 6.2: Voltage Regulator Operator-Controlled Pushbuttons

Pushbutton Name	Function
SETTINGS	Displays active group settings
METER	Displays fundamental metering report
OPERATION COUNT	Displays tap report
VOLTAGE LIMIT	Displays voltage limit settings
LINE DROP COMP.	Displays line drop compensation settings
HARMONICS	Displays harmonic metering report
DEMAND	Displays demand metering report
LOCAL/REMOTE	Selects LOCAL or REMOTE device operation
AUTO/MANUAL	Selects AUTO or MANUAL device operation
RAISE	Allows manual raising of tap
LOWER	Allows manual lowering of tap

6.1.3 Voltage Regulator Control I/O List

The I/O contacts designated for the voltage regulator control have been assigned based on settings received from SDG&E and the test requirements.

6.1.4 RTDS to Vendor B Amplifier Low-Level Test Interface

The RTDS simulates the power system signal and converts the digital signals to low-level analog signals that are ready to be applied to the Vendor B amplifier. The RTDS analog outputs, consisting of voltage and current outputs, are connected to the amplifier via a DB-15 cable. Figure 6.2 illustrates the analog outputs from the RTDS to the amplifier via the gigabit transceiver analog output (GTAO) card. channels 1 through 3 and channels 7 through 9 are reserved for the source-side and load-side voltages, respectively. The device can be programmed to amplify the low-level signals to the desired voltage and current levels for testing. The output of the amplifier is connected to the voltage regulator control. As illustrated in Figure 6.2, 69G1A, 69G1B, and 69G1C are the phase voltages of the load side and 69G2A, 69G2B, and 69G2C are the phase voltages of the source side of the voltage regulator C1215-69G.

The voltage regulator control digital outputs used for voltage control are given in Table 6.3.

Figure 6.3 shows the mapping for the voltage regulator digital inputs (raise, lower, and block) via the gigabit transceiver front-panel interface (GTFPI) card.

Note: ABC phase rotation is considered.

Table 6.3: Voltage Regulator Control I/O List

Output Contact	Function
OUT102	Raise Phase A
OUT103	Lower Phase A
OUT104	Block Phase A
OUT102	Raise Phase B
OUT103	Lower Phase B
OUT104	Block Phase B
OUT102	Raise Phase C
OUT103	Lower Phase C
OUT104	Block Phase C

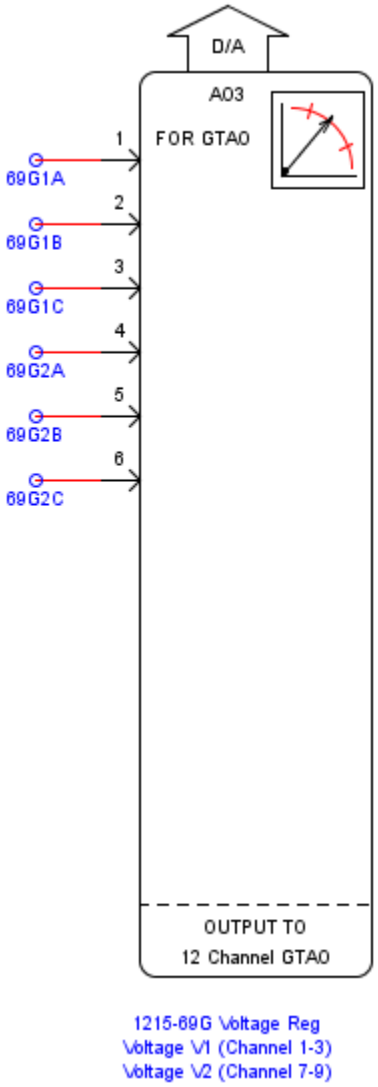


Figure 6.2: RTDS to Vendor B Amplifier Interface

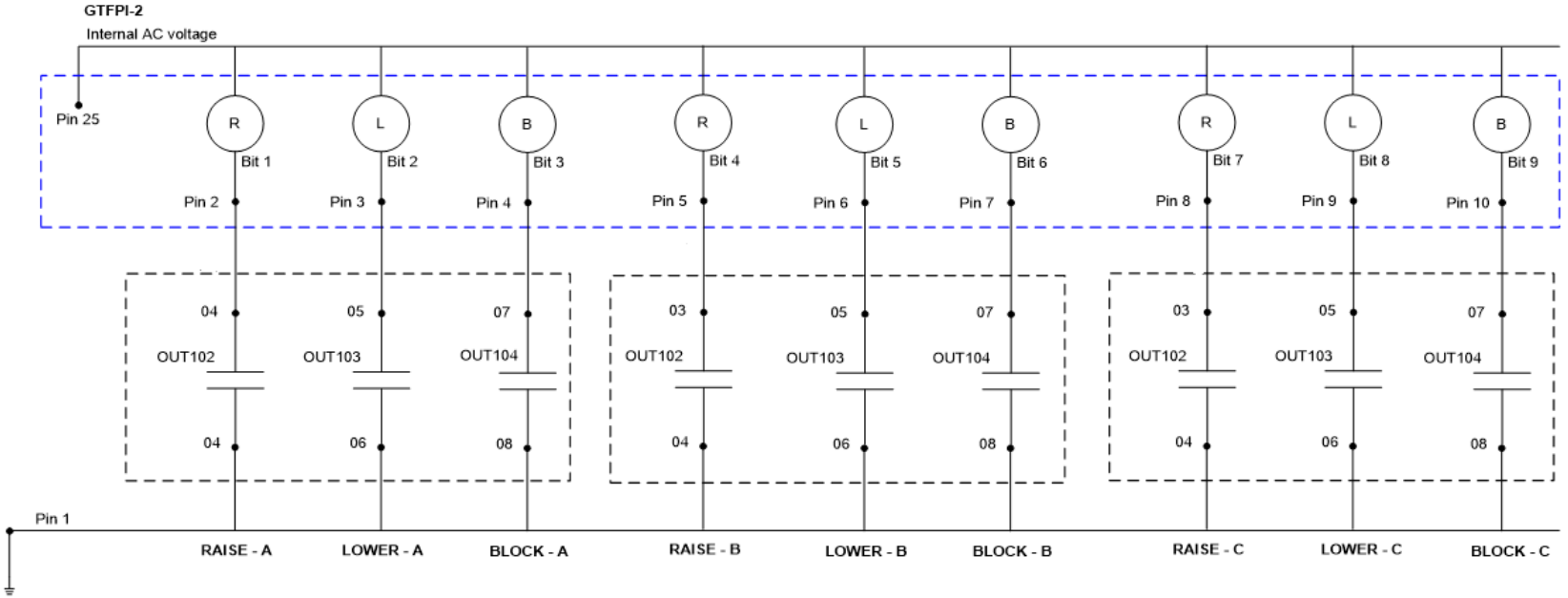


Figure 6.3: Raise, Lower, and Block Digital Input Wiring

6.1.5 Vendor B Amplifier to Voltage Regulator Control Test Interface

Figure 6.4 provides detailed information on the amplifier to the voltage regulator external test wiring. Figure 6.5 shows the internal wiring of the voltage regulator.

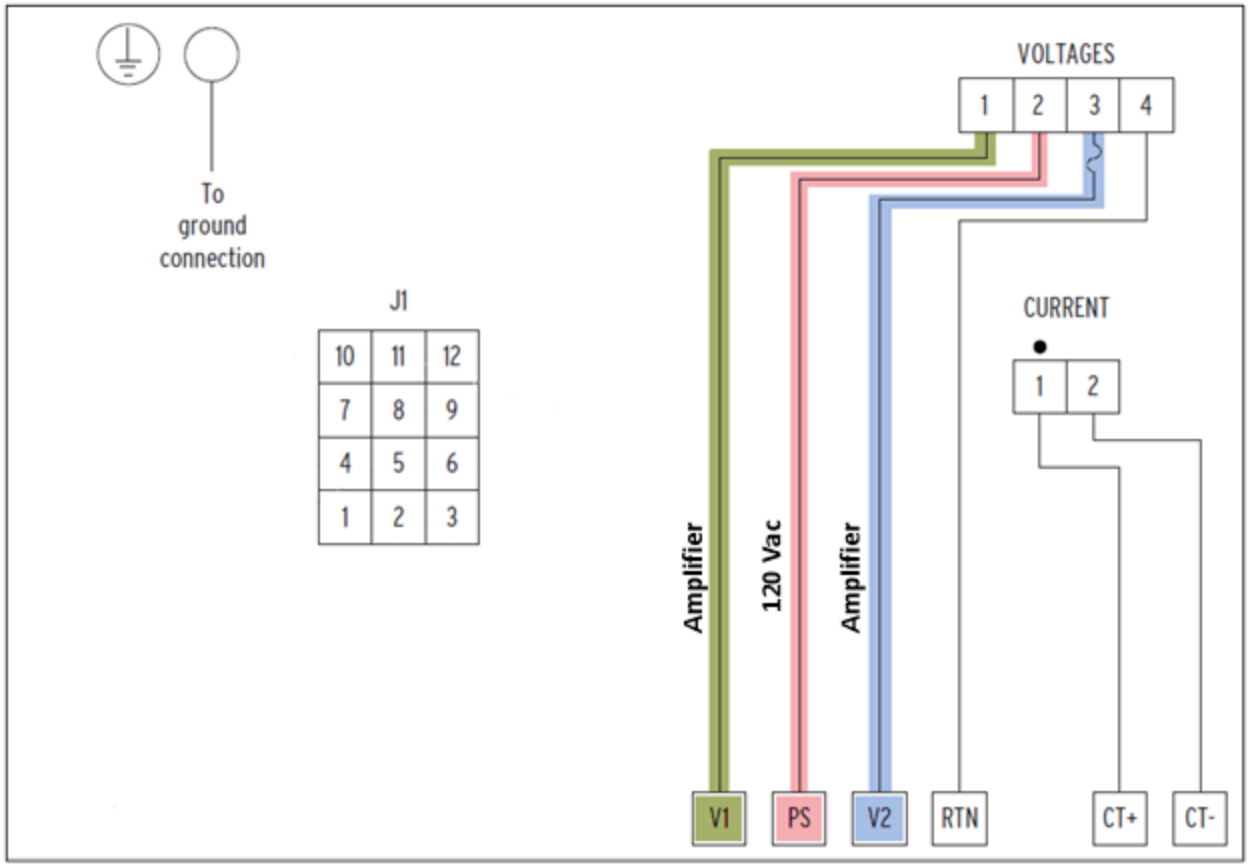


Figure 6.4: Voltage Regulator External Connection Diagram

For this testing:

- A 120 Vac power source is connected to PS.
- The load-side voltage (VL) is connected to V1.
- The source-side voltage (VS) is connected to V2.
- The secondary CT currents are connected to CT+ and CT–.
- The retrofit cable harness connector (J1) will not be used.

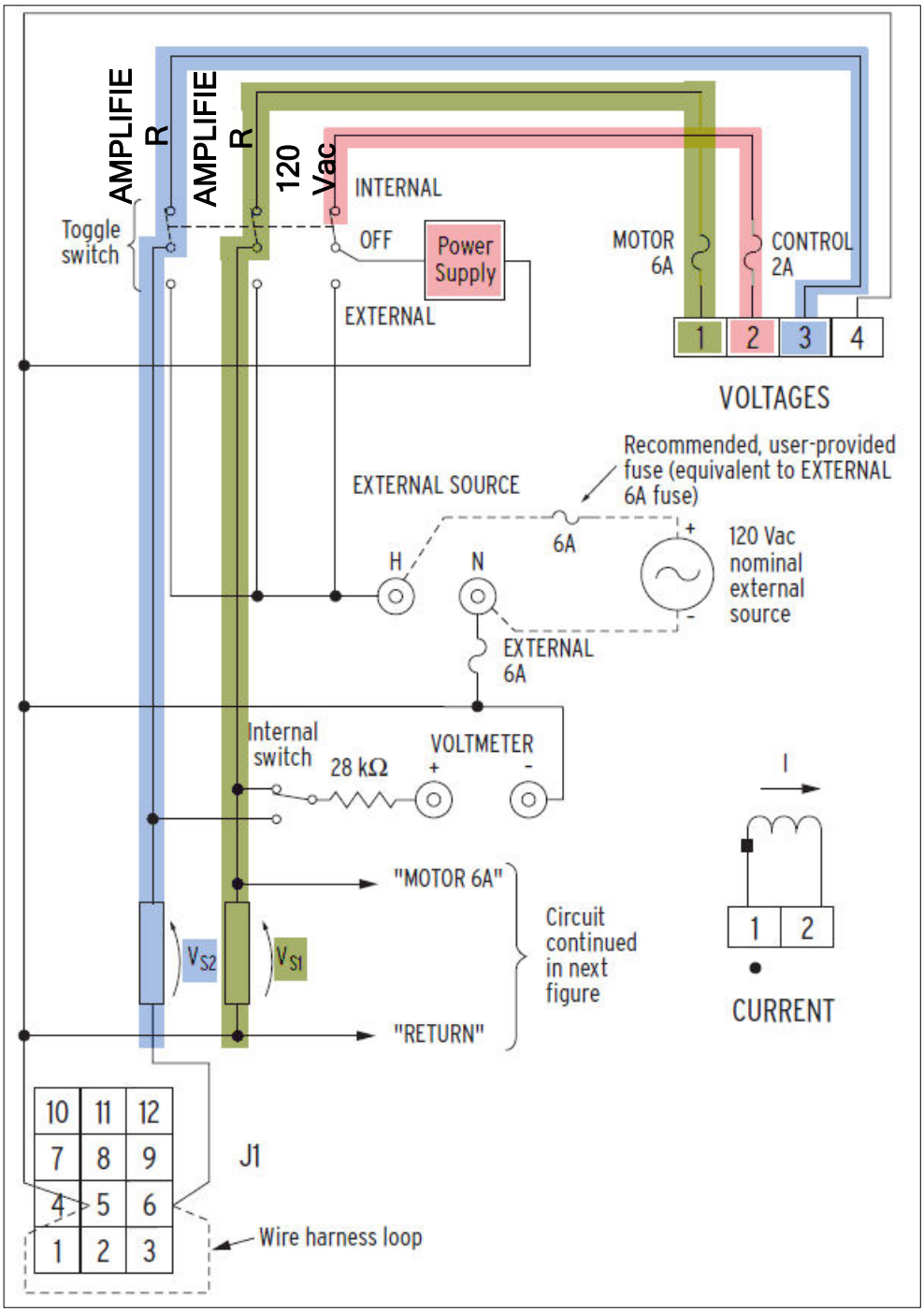


Figure 6.5: Voltage Regulator Internal Connection Diagram

To inject VS (source-side voltage) and VL (load-side voltage) from the amplifier, follow these instructions:

Step 1. Switch the control power in the front panel to Internal mode.

Step 2. Connect 120 Vac external source to V1 and G. This step will turn on the relay.

Step 3. Check to see if the relay turns on.

Step 4. Connect the voltage source from the amplifier to V1. This step will inject VL from the amplifier to the voltage regulator.

Step 5. Connect the voltage source from the amplifier to V2. This step will inject VS from the amplifier to the voltage regulator.

Step 6. Check to see if both VS and VL measurements from the relay match the amplifier voltage output.

The VS1 and VS2 generated are the variables used for the voltage regulation. VS1 corresponds to the load-side voltage and VS2 corresponds to the source-side voltage. Based on the inputs from VS1 and VS2 and the voltage range between which the voltage must be regulated, certain output contacts are triggered to raise or lower the voltage. The tap slider is shifted up or down based on the operation.

Figure 6.6 is an example case that shows the voltage profile and tap-changing positions for a voltage raise operation on a 32-tap voltage regulator unit.

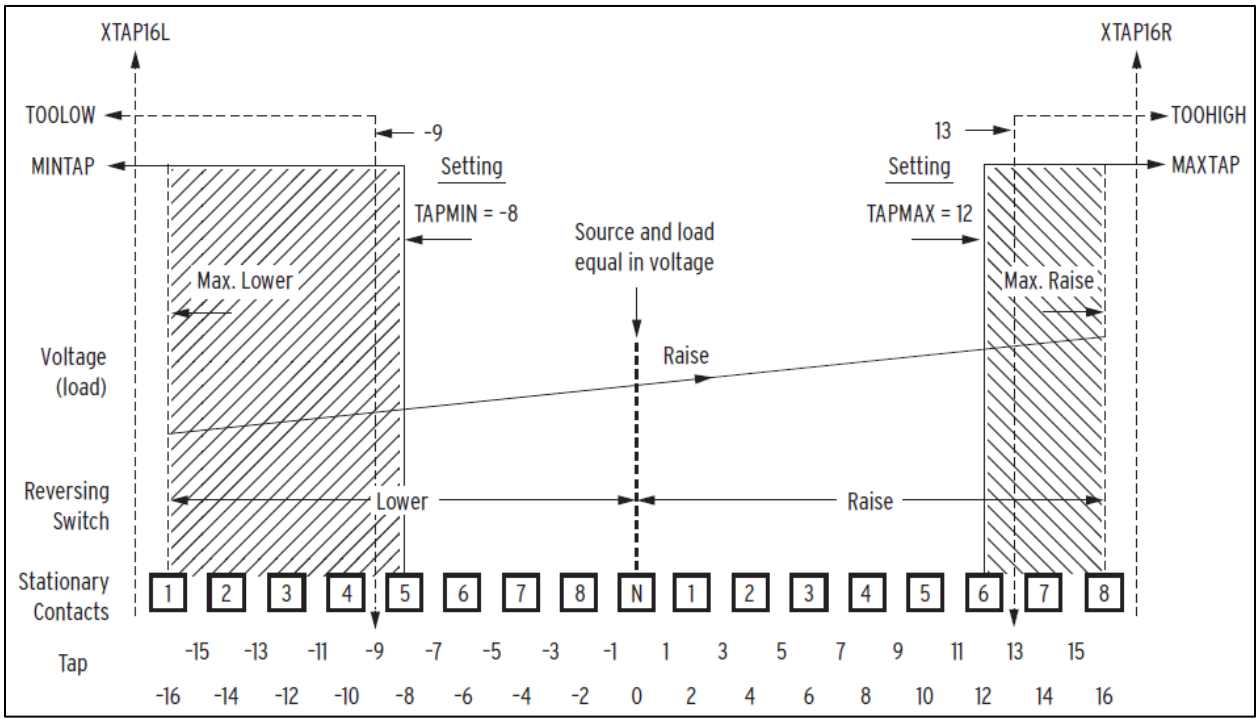


Figure 6.6: Voltage Profile Plot of a Continual Raise Operation

Notes:

- The device word bits TAPMAX and TAPMIN are the boundary tap positions for the voltage regulator control.
- The device word bit TOOLOW asserts to a logical 1 when the tap is at a TAPMIN –1 or a lower tap value.
- The device word bit TOOHIGH asserts to a logical 1 when the tap is at a TAPMAX –1 or a higher tap value.

- The device word bit XTAP16L asserts momentarily to a logical 1 when the tap value attempts to go lower than TAP = –16.
- The device word bit XTAP16R asserts momentarily to a logical 1 when the tap value attempts to go higher than TAP = 16.

6.2 OPERATING MODES

The voltage regulator control has several operating modes to accommodate different operating conditions and applications. The automatic modes of operation dictate whether the voltage regulator control will regulate voltage in the forward or reverse direction. The different modes of operation are as follows:

1. Locked Forward Mode (LOCKFWD): Power flow is expected to always be in the forward direction (normal load side).

2. Locked Reverse Mode (LOCKREC): Power flow is expected to always be in the reverse direction (normal source side).

3. Idle Reverse Mode (IDLEREV): Power flow is expected to always be in the forward direction; however, no voltage regulation should occur if the power flow is indeterminate, such as a no-load condition.

4. Bidirectional Mode (BIDIR): Power flow varies, alternatively operating in the forward and reverse directions.

5. Cogeneration Mode (COGEN): Cogeneration/independent generation unit is on the normal load side and the power flow varies, alternatively operating in the forward and reverse directions.

The voltage regulator controls in the SDG&E circuits are set to the locked forward operating mode. Depending on the operating mode, the voltage regulator generates output control commands based on the voltage it sees on the load and source side.

1. Raise Tap (RAISESV): Tap to be raised because the current tap is too low (TOOLOW asserts).

2. Lower Tap (LOWERSV): Tap to be lowered because the current tap is too high (TOOHIGH asserts).

3. Inhibit Tap (INHIBITSV): The INHIBITSV asserts when the voltage is out of band. It then deasserts and the timing to tap restarts from the beginning.

4. Block Tap (BLOCKSV): The block tap operates similar to the INHIBITSV Relay Word bit. However, when the BLOCKSV asserts, the timing to tap continues with the present timer. No tapping occurs when the timer times out (a pending tap condition exists). Then, if the voltage is still out of band when it deasserts, a tap occurs immediately for this pending tap condition.

6.3 TEST PROCEDURE

The following is the procedure carried out during the testing process:

Step 1. Connect the RTDS I/O module to the amplifier as described in Section 6.1.4.

Step 2. Connect the amplifier to the voltage regulator.

Step 3. Modify the voltage regulator control settings to reflect the tap and voltage limits, as provided by SDG&E.

Step 4. Run the RTDS model and verify accuracy of the I/O across all devices. Follow the instructions described in Section 6.1.5 for the amplifier connected to the voltage regulator control.

Step 5. Run the RTDS model on varying loads based on the load profile provided by SDG&E and observe the operation of the voltage regulator.

According to recommendations from SDG&E, the load was increased considerably to best simulate the voltage regulator operation. The modified load profile was essentially the original load profile with each load point increased to three times the actual load.

Step 6. Observe the voltage profile on the RTDS RunTime interface for each voltage regulator operation.

Step 7. Analyze each voltage regulator operation and suggest steps to improve the voltage profile, if required.

6.4 VOLTAGE REGULATOR TEST

The functional testing of the voltage regulators was performed on the desert-rural test circuit. The desert-rural circuit was chosen for these tests since it has existing voltage regulators installed. The analysis and understanding of the voltage regulator operation, as a stand-alone device for correcting the voltage profile, will aid in developing the voltage support coordination scheme using multiple devices in Section 10.

This circuit has two voltage regulator banks, as shown in Figure 6.7. For this study, the voltage regulators 1215-69G were considered because of their proximity to the source and the number of loads available on their load terminals.

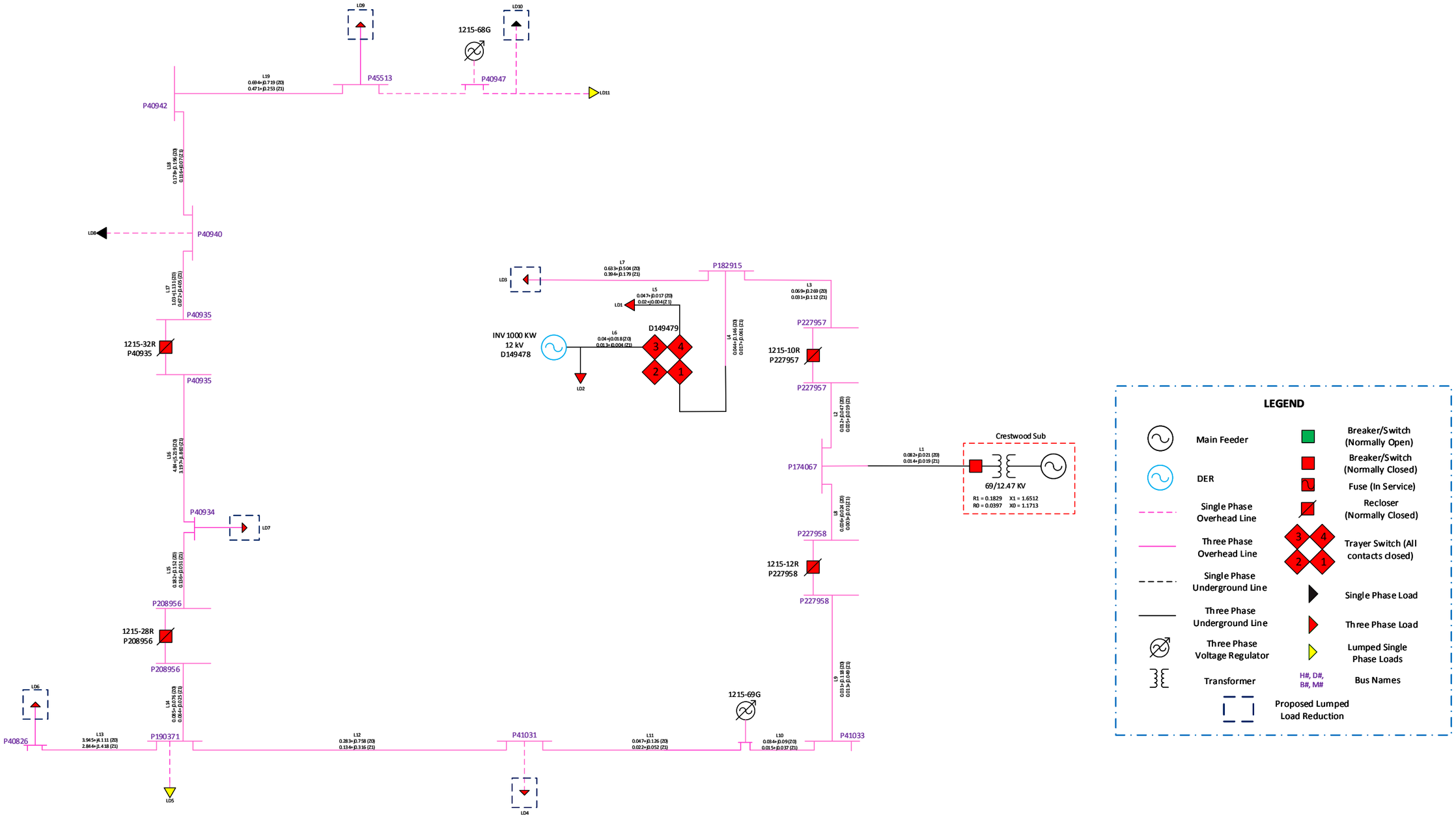


Figure 6.7: Simplified One-Line Drawing of Desert-Rural Test Circuit

6.5 VOLTAGE REGULATOR RTDS MODEL

Figure 6.8 shows the voltage regulator block and the logic for the voltage regulator, which is modeled in RSCAD.

The voltage regulator has input terminals connected to the source side and output terminals connected to the load side of the circuit. The device internal logic is shown in Figure 6.9. It consists of single-phase voltage sources connected to each phase, controlled by a regulated voltage. The voltage at the source side is sent to the externally connected voltage regulator. The voltage regulator performs the necessary calculations to determine whether a raise or a lower tap operation should be carried out. The corresponding tap operation is sent to the RTDS and based on the tap input received, the internal tap is suitably raised or lowered and fed to the single-phase voltage sources. This regulates the load voltage and ensures that the voltage stays within the specified operation band.

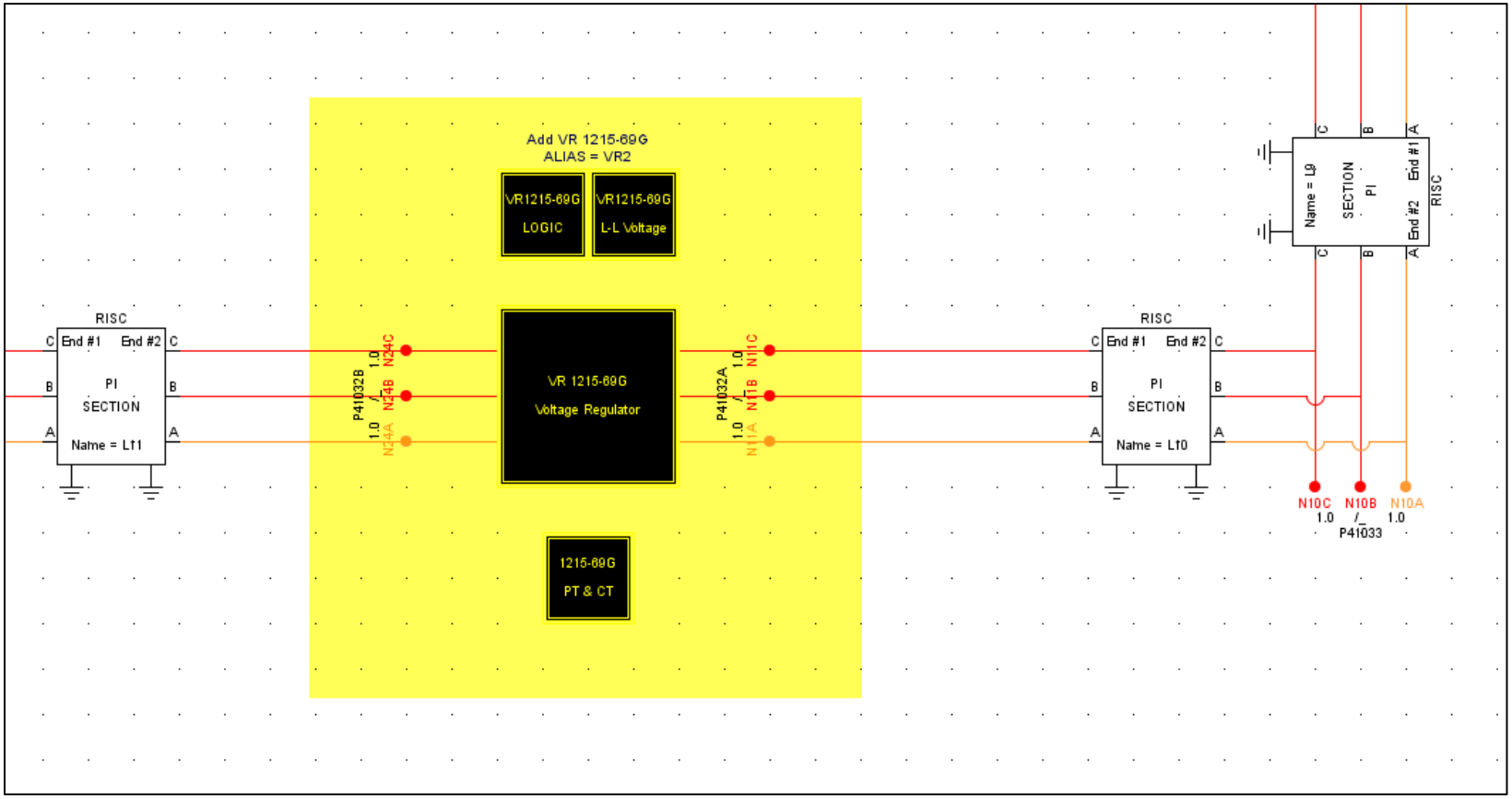


Figure 6.8: Voltage Regulator RTDS Block

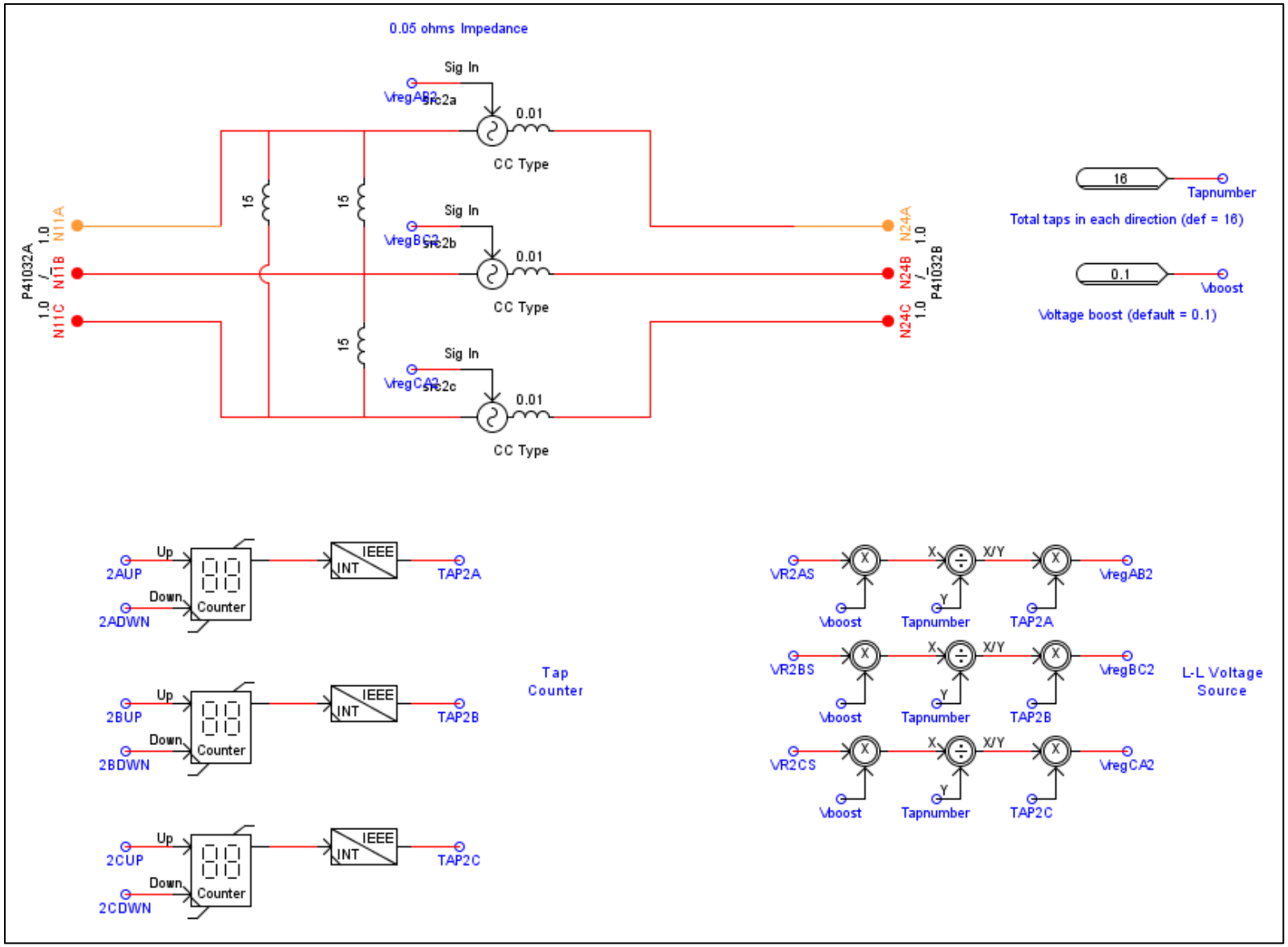


Figure 6.9: Voltage Regulator Internal Logic

6.6 VOLTAGE REGULATOR SETTINGS

The voltage regulator was set based on the standards specified by SDG&E. The following are the relevant settings that were used in the device:

CTR → 60

PTR → 1000

PT secondary voltage → 120 V

Tap changer type → COOPER

Operating mode → locked forward

Maximum tap number → 16

Minimum tap number → –16

Forward center band → 120 V

Forward bandwidth → 2 V

Forward time delay → 10 s

Maximum voltage → 130 V

Minimum voltage → 110 V

A detailed list of all voltage regulator settings is in Appendix D.

Figure 6.10 illustrates the voltage band setting for a voltage regulator. The device regulates the load-side voltage within these parameters. The device does not operate when the voltage is within the In Band voltage range. When the load voltage increases to the high-voltage band because of certain conditions such as loss of load or source fluctuations, the voltage regulator raises the tap to bring down the voltage to within the In Band voltage range. When the load voltage drops to the low-voltage band, the device raises the tap to bring the voltage within the In Band voltage range. Additionally, when the voltage goes beyond the maximum or minimum voltage limit, the device blocks all tap operations and stays idle until the voltage comes back to the device operating band. SDG&E recommends a ±5 percent voltage band over the center voltage band of 120 V. This equates to an In Band between 114 V and 126 V.

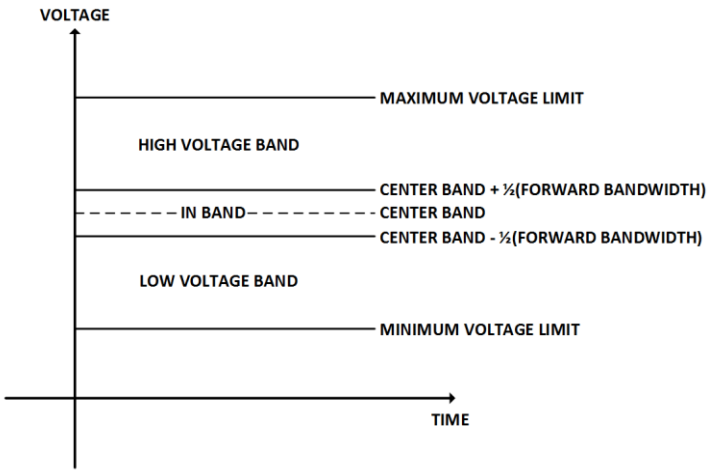


Figure 6.10: Voltage Regulator Voltage Band Setting

6.7 RTDS TEST ASSUMPTIONS

The following are the assumptions made for the RTDS voltage regulator functional tests:

- The forward bandwidth was set to 2 V (±0.8 percent) to better simulate voltage regulator operations.
- The 24-hour load profile provided by SDG&E was condensed to a 1-hour load profile for a realistic test study.

6.8 TEST SCENARIOS

6.8.1 Auto and Remote Toggle – From Local Control

Table 6.4: Auto and Remote Toggle – Local Control

Objective: Verify appropriate indication for AUTO/REMOTE operating mode.					
Specific instruction: AUTO/REMOTE toggle allowed by **AUTO** and **REMOTE** pushbutton in LOCAL mode. Carry out Test Action 1, observe corresponding results. Move on to Step 2.					
Negative test: Modes do not switch between LOCAL/MANUAL and AUTO/REMOTE.					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. Voltage regulator in MANUAL mode. **MANUAL** LED is ON.	1. Press **AUTO/MANUAL** pushbutton. 2. Press **AUTO/MANUAL** pushbutton.	1.a. **AUTO** LED – ON 1.b. **MANUAL** LED – OFF 1.c. Voltage Regulator in AUTO mode 2.a. **AUTO** LED – OFF 2.b. **MANUAL** LED – ON 2.c. Voltage regulator in MANUAL mode	1. Voltage regulator switches to AUTO mode successfully. 2. Voltage regulator switches to MANUAL mode successfully.	Y	
2. Voltage regulator in MANUAL mode. **MANUAL** LED is ON.	1. Press **REMOTE/LOCAL** pushbutton. 2. Press **REMOTE/LOCAL** pushbutton.	1.a. **REMOTE** LED – ON 1.b. **LOCAL** LED – OFF 1.c. Voltage regulator in REMOTE mode 2.a. **REMOTE** LED – OFF 2.b. **LOCAL** LED – ON 2.c. Voltage regulator in LOCAL mode	1. Voltage regulator switches to REMOTE mode successfully. 2. Voltage regulator switches to LOCAL mode successfully.	Y	
Test notes: The voltage regulator may be placed in Automatic mode when there are no lockout conditions and all three-phase voltages are healthy. Observe system voltage profile after the switching operation.					

The Sequential Events Recorder (SER) report for the Auto and Remote Toggle tests carried out as outlined in Table 6.4 is illustrated in Figure 6.11, Figure 6.12, and Figure 6.13. The voltage regulators performed switching between AUTO and REMOTE modes successfully per the test specifications.

#	DATE	TIME	ELEMENT	STATE
9	01/18/2000	09:55:34.628	SER Archive Cleared	
8	01/18/2000	09:56:11.047	MANUAL	Asserted
7	01/18/2000	09:56:11.047	AUTO	Deasserted
6	01/18/2000	09:56:11.063	LOCAL	Asserted
5	01/18/2000	09:56:11.063	REMOTE	Deasserted
4	01/18/2000	09:56:17.547	MANUAL	Deasserted
3	01/18/2000	09:56:17.547	AUTO	Asserted
2	01/18/2000	09:56:18.597	LOCAL	Deasserted
1	01/18/2000	09:56:18.597	REMOTE	Asserted

=>

Figure 6.11: Test Scenario 3.7.1. Phase A Voltage Regulator SER

#	DATE	TIME	ELEMENT	STATE
9	01/18/2000	09:22:49.783	SER Archive Cleared	
8	01/18/2000	09:56:55.422	MANUAL	Asserted
7	01/18/2000	09:56:55.422	AUTO	Deasserted
6	01/18/2000	09:56:55.439	LOCAL	Asserted
5	01/18/2000	09:56:55.439	REMOTE	Deasserted
4	01/18/2000	09:57:00.972	MANUAL	Deasserted
3	01/18/2000	09:57:00.972	AUTO	Asserted
2	01/18/2000	09:57:02.789	LOCAL	Deasserted
1	01/18/2000	09:57:02.789	REMOTE	Asserted

=>

Figure 6.12: Test Scenario 3.7.1. Phase B Voltage Regulator SER

#	DATE	TIME	ELEMENT	STATE
9	01/18/2000	09:23:28.909	SER Archive Cleared	
8	01/18/2000	09:57:07.263	MANUAL	Asserted
7	01/18/2000	09:57:07.263	AUTO	Deasserted
6	01/18/2000	09:57:07.280	LOCAL	Asserted
5	01/18/2000	09:57:07.280	REMOTE	Deasserted
4	01/18/2000	09:57:10.330	MANUAL	Deasserted
3	01/18/2000	09:57:10.330	AUTO	Asserted
2	01/18/2000	09:57:11.064	LOCAL	Deasserted
1	01/18/2000	09:57:11.064	REMOTE	Asserted

=>

Figure 6.13: Test Scenario 3.7.1. Phase C Voltage Regulator SER

6.8.2 Automatic Voltage Regulation – Voltage Raise/Lower Operation

Voltage regulation is performed by the voltage regulator within its voltage band settings. The device must be set in AUTO mode for voltage regulation. The voltage regulator detects voltages that fall outside the voltage regulation band and subsequently raises or lowers tap to bring the voltage within specified limits. The voltages specified in Table 6.5 and Table 6.6 indicate the CT secondary voltages.

Table 6.5: High-Voltage Lower Tap Operation

Objective: Verify regulator lowers tap for high-voltage conditions.					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. System with nominal voltage and current conditions: VA = 120 V ∠0° VB = 120 V ∠–120° VC = 120 V ∠+120° 2. Voltage regulator in AUTO and REMOTE modes. 3. Voltage regulation enabled. 4. Initial tap setting.	1. Raise test set voltage VA = 121 V ∠0° VB = 121 V ∠–120° VC = 121 V ∠+120°	1.a. **HIGH BAND** LED blinks yellow. 1.b. Lower Tap operation initiated. 1.c. **IN BAND** LED blinks green.	The **HIGH BAND** LED turns yellow as expected. LOWER Word bit initiated by the relay resulting in tap lowering.	Y	
1. System with nominal voltage and current conditions: VA = 120 V ∠0° VB = 120 V ∠–120° VC = 120 V ∠+120° 2. Voltage regulator in AUTO and REMOTE modes. 3. Voltage regulation enabled. 4. Initial tap setting.	1. Raise test set voltage VA = 128 V ∠0° VB = 128 V ∠–120° VC = 128 V ∠+120°	1.a. **HIGH BAND** LED blinks yellow. 1.b. Lower Tap operation initiated. 1.c. Voltage verified or previous tap operation. 1.d. Next Lower Tap operation initiated after the forward tap delay. 1.e. Steps 1.c. and 1.d. repeat until load voltage is In Band. 1.f. **IN BAND** LED blinks green.	The voltage regulator operated as desired for a high band, with checks at each tap operation until the voltage was In Band.	Y	
Test notes: Voltage regulator operation is verified for each phase. Observe system voltage profile after the switching operation.					

Refer to Figure 6.14 through Figure 6.19 for combined high- and low-voltage tap operations.

Table 6.6: Low-Voltage Raise Tap Operation

Objective: Verify regulator raises tap for low-voltage conditions.					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. System with nominal voltage and current conditions: VA = 120 V ∠0° VB = 120 V ∠–120° VC = 120 V ∠+120° 2. Voltage regulator control in AUTO and REMOTE modes. 3. Voltage regulation enabled. 4. Initial tap setting.	1. Lower test set voltage VA = 119 V ∠0° VB = 119 V ∠–120° VC = 119 V ∠+120°	1.a. **LOW BAND** LED blinks yellow. 1.b. Raise Tap operation initiated. 1.c. **IN BAND** LED blinks green.	The **LOW BAND** LED turns yellow as expected. RAISE Word bit initiated by the relay resulting in tap lowering.	Y	
1. System with nominal voltage and current conditions: VA = 120 V ∠0° VB = 120 V ∠–120° VC = 120 V ∠+120° 2. Voltage regulator control in AUTO and REMOTE modes. 3. Voltage regulation enabled. 4. Initial tap setting.	1. Lower test set voltage VA = 112 V ∠0° VB = 112 V ∠–120° VC = 112 V ∠+120°	1.a. **LOW BAND** LED blinks yellow. 1.b. Raise Tap operation initiated. 1.c. Voltage verified for previous tap operation. 1.d. Next Raise Tap operation initiated after the forward tap delay. 1.e. Steps 1.c. and 1.d. repeat until load voltage is In Band. 1.f. **IN BAND** LED blinks green.	The voltage regulator operated as desired for a low band, with checks at each tap operation until the voltage was In Band.	Y	
Test notes: Voltage regulator operation is verified for each phase. Observe system voltage profile after the switching operation.					

Figure 6.14 through Figure 6.19 illustrate voltage raise and lower operations performed by the voltage regulators and their respective SER data. It was observed that with an increase in load, there was a significant voltage drop in the system. The voltage regulators detected a drop-in voltage beyond the normal operating band (In Band) and correspondingly raised the regulator tap in steps to bring back the voltage to the normal operating band. The time stamp with the voltage reading indicates the point at which the voltage is In Band. The load was not decreased, resulting in the system voltage increasing to the high-voltage band of the voltage regulator. The voltage regulators lowered the regulator tap in steps to bring the voltage back to the normal operating band.

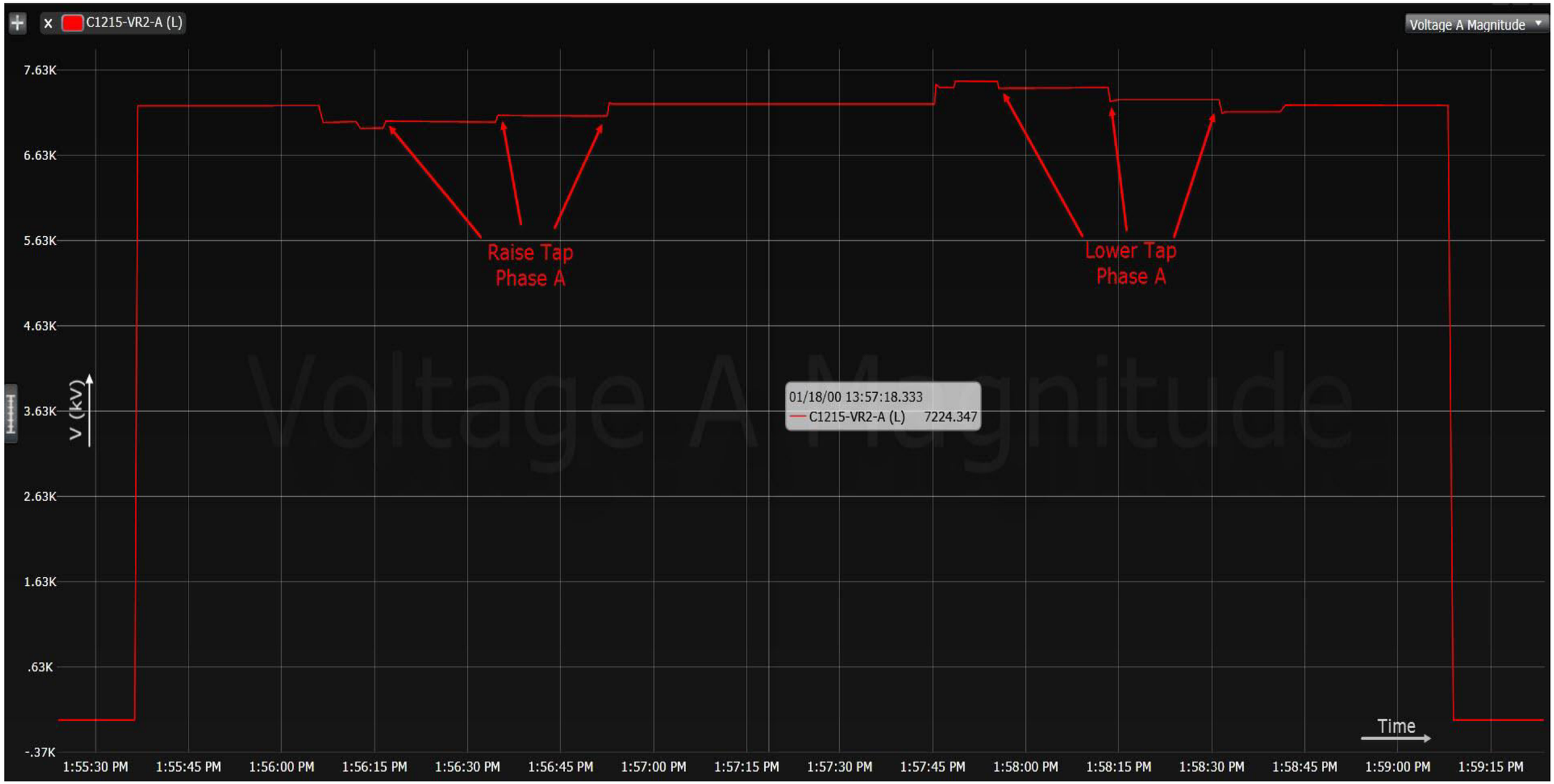
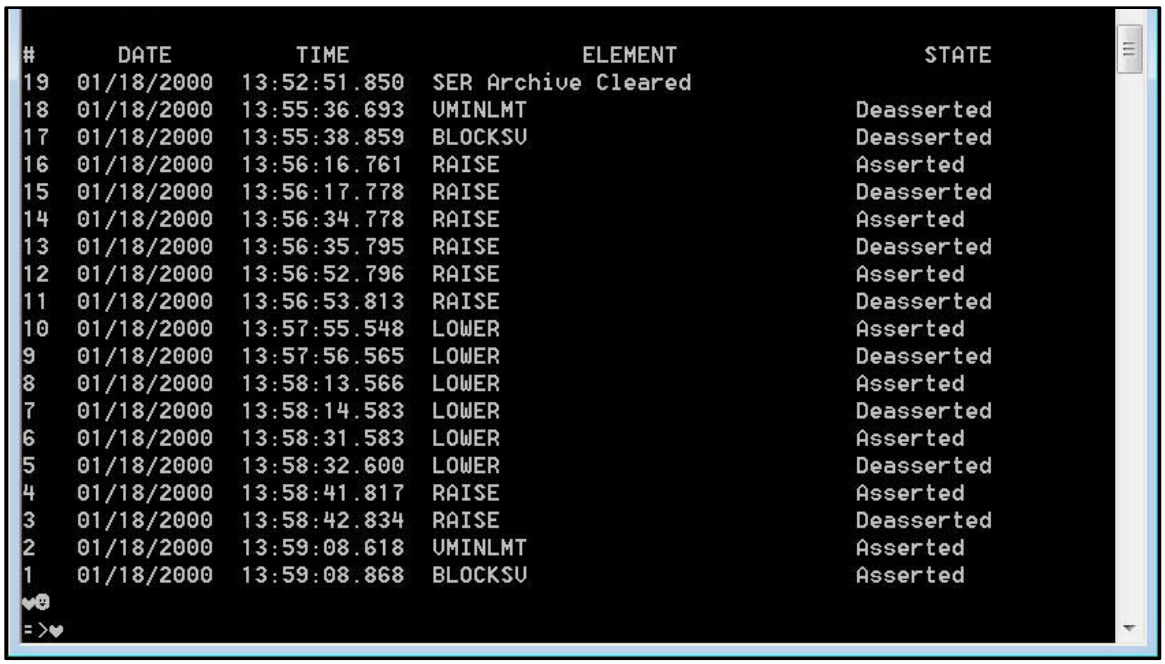


Figure 6.14: Test Scenario 3.7.2. Phase A Voltage Regulator Output Voltage Waveform



#	DATE	TIME	ELEMENT	STATE
19	01/18/2000	13:52:51.850	SER Archive Cleared	
18	01/18/2000	13:55:36.693	VMINLMT	Deasserted
17	01/18/2000	13:55:38.859	BLOCKSV	Deasserted
16	01/18/2000	13:56:16.761	RAISE	Asserted
15	01/18/2000	13:56:17.778	RAISE	Deasserted
14	01/18/2000	13:56:34.778	RAISE	Asserted
13	01/18/2000	13:56:35.795	RAISE	Deasserted
12	01/18/2000	13:56:52.796	RAISE	Asserted
11	01/18/2000	13:56:53.813	RAISE	Deasserted
10	01/18/2000	13:57:55.548	LOWER	Asserted
9	01/18/2000	13:57:56.565	LOWER	Deasserted
8	01/18/2000	13:58:13.566	LOWER	Asserted
7	01/18/2000	13:58:14.583	LOWER	Deasserted
6	01/18/2000	13:58:31.583	LOWER	Asserted
5	01/18/2000	13:58:32.600	LOWER	Deasserted
4	01/18/2000	13:58:41.817	RAISE	Asserted
3	01/18/2000	13:58:42.834	RAISE	Deasserted
2	01/18/2000	13:59:08.618	VMINLMT	Asserted
1	01/18/2000	13:59:08.868	BLOCKSV	Asserted

=>

Figure 6.15: Test Scenario 3.7.2. Phase A Voltage Regulator SER

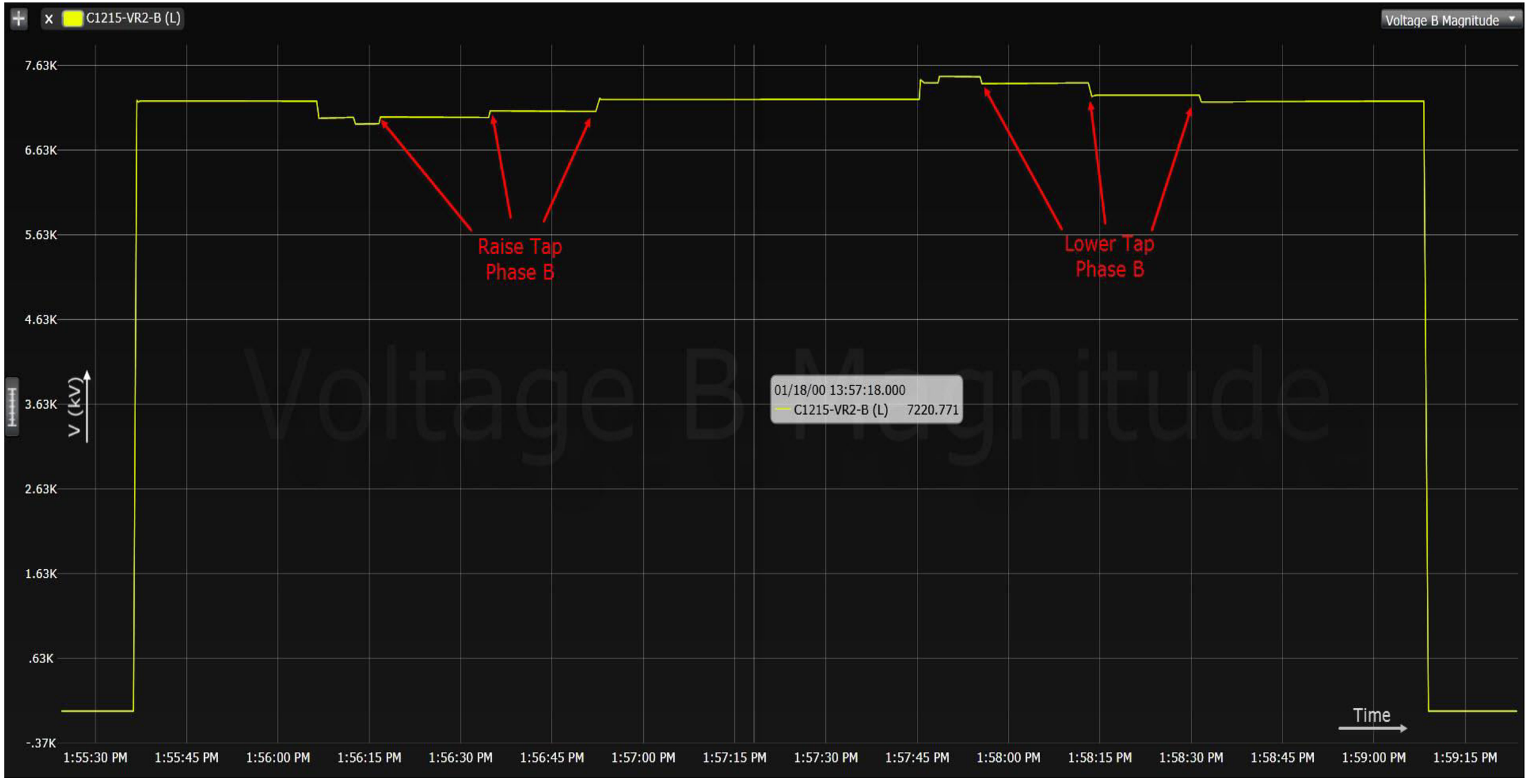
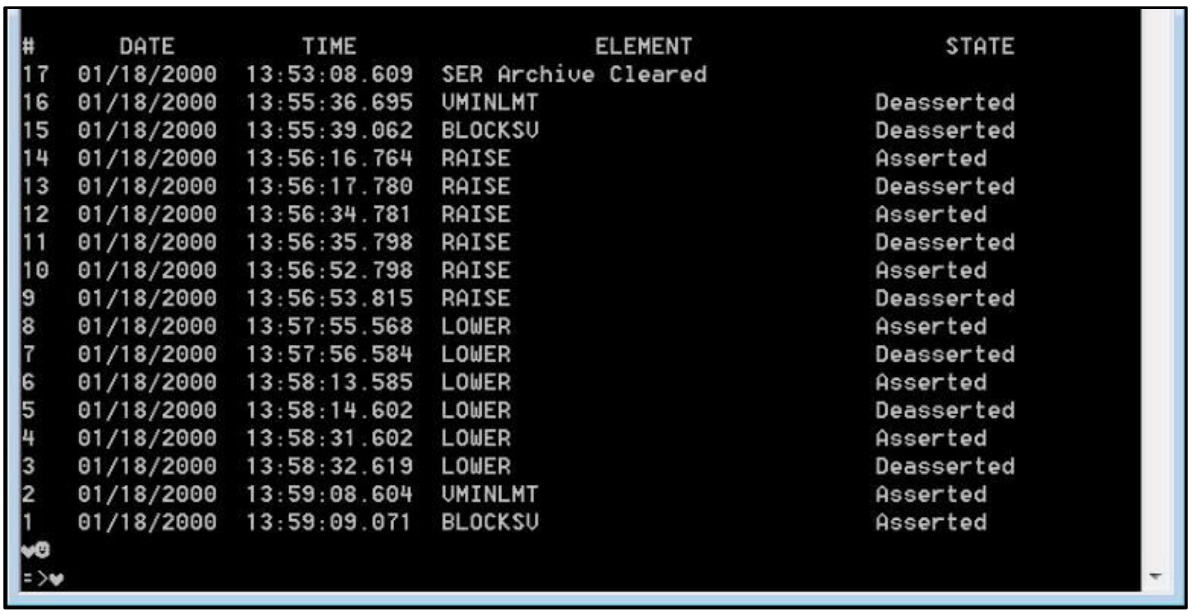


Figure 6.16: Test Scenario 3.7.2. Phase B Voltage Regulator Output Voltage Waveform



#	DATE	TIME	ELEMENT	STATE
17	01/18/2000	13:53:08.609	SER Archive Cleared	
16	01/18/2000	13:55:36.695	VMINLMT	Deasserted
15	01/18/2000	13:55:39.062	BLOCKSV	Deasserted
14	01/18/2000	13:56:16.764	RAISE	Asserted
13	01/18/2000	13:56:17.780	RAISE	Deasserted
12	01/18/2000	13:56:34.781	RAISE	Asserted
11	01/18/2000	13:56:35.798	RAISE	Deasserted
10	01/18/2000	13:56:52.798	RAISE	Asserted
9	01/18/2000	13:56:53.815	RAISE	Deasserted
8	01/18/2000	13:57:55.568	LOWER	Asserted
7	01/18/2000	13:57:56.584	LOWER	Deasserted
6	01/18/2000	13:58:13.585	LOWER	Asserted
5	01/18/2000	13:58:14.602	LOWER	Deasserted
4	01/18/2000	13:58:31.602	LOWER	Asserted
3	01/18/2000	13:58:32.619	LOWER	Deasserted
2	01/18/2000	13:59:08.604	VMINLMT	Asserted
1	01/18/2000	13:59:09.071	BLOCKSV	Asserted

Figure 6.17: Test Scenario 3.7.2. Phase B Voltage Regulator SER

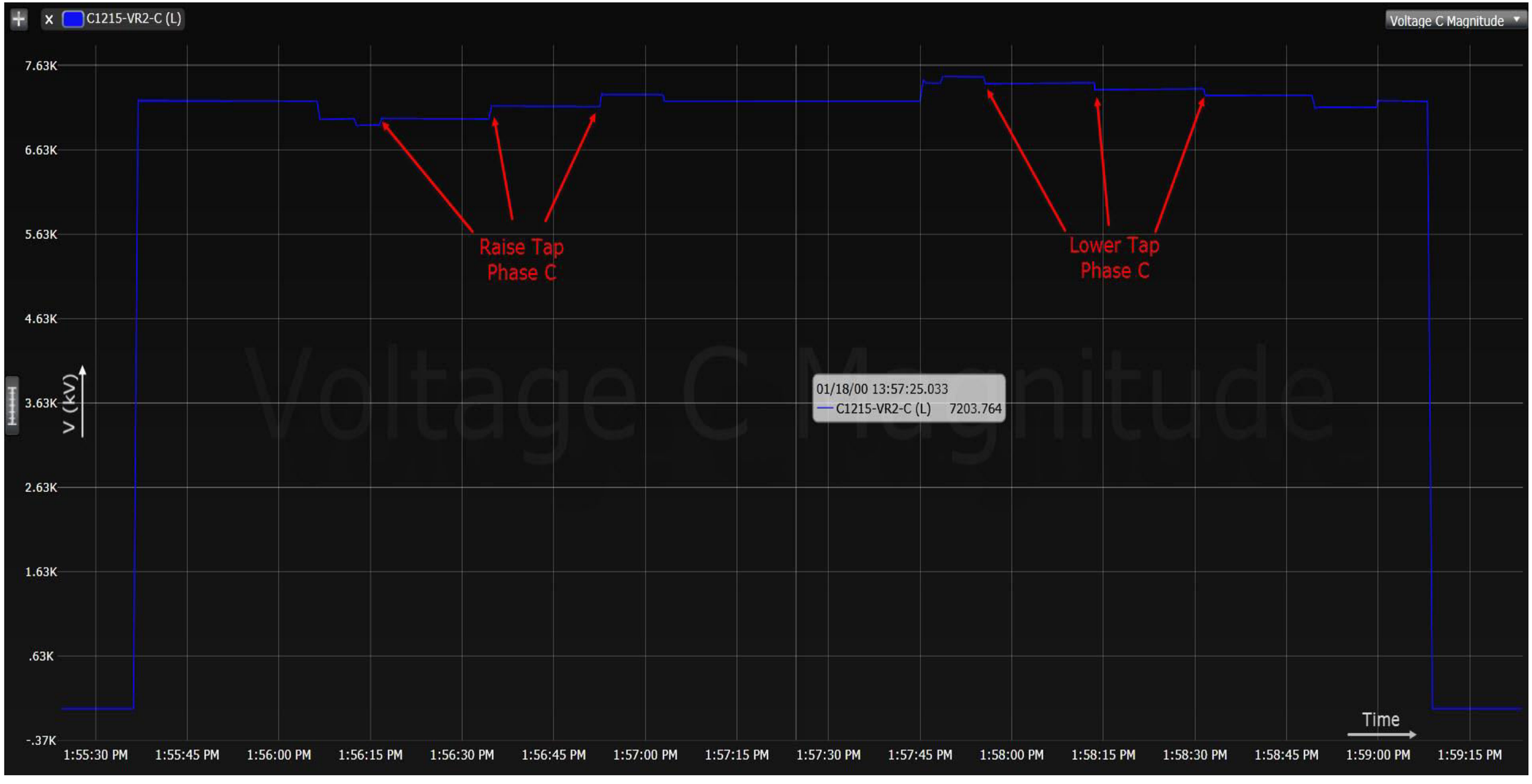
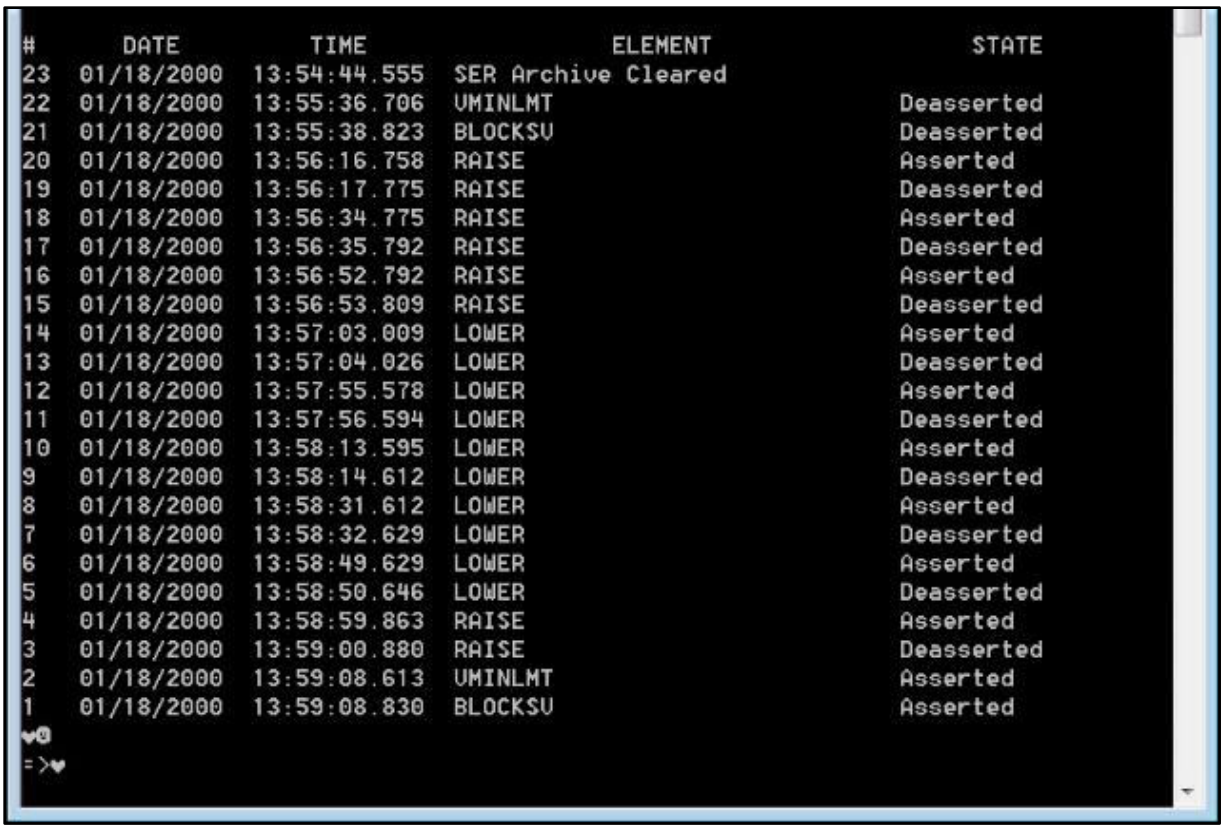


Figure 6.18: Test Scenario 3.7.2. Phase C Voltage Regulator Output Voltage Waveform



#	DATE	TIME	ELEMENT	STATE
23	01/18/2000	13:54:44.555	SER Archive Cleared	
22	01/18/2000	13:55:36.706	VMINLMT	Deasserted
21	01/18/2000	13:55:38.823	BLOCKSV	Deasserted
20	01/18/2000	13:56:16.758	RAISE	Asserted
19	01/18/2000	13:56:17.775	RAISE	Deasserted
18	01/18/2000	13:56:34.775	RAISE	Asserted
17	01/18/2000	13:56:35.792	RAISE	Deasserted
16	01/18/2000	13:56:52.792	RAISE	Asserted
15	01/18/2000	13:56:53.809	RAISE	Deasserted
14	01/18/2000	13:57:03.009	LOWER	Asserted
13	01/18/2000	13:57:04.026	LOWER	Deasserted
12	01/18/2000	13:57:55.578	LOWER	Asserted
11	01/18/2000	13:57:56.594	LOWER	Deasserted
10	01/18/2000	13:58:13.595	LOWER	Asserted
9	01/18/2000	13:58:14.612	LOWER	Deasserted
8	01/18/2000	13:58:31.612	LOWER	Asserted
7	01/18/2000	13:58:32.629	LOWER	Deasserted
6	01/18/2000	13:58:49.629	LOWER	Asserted
5	01/18/2000	13:58:50.646	LOWER	Deasserted
4	01/18/2000	13:58:59.863	RAISE	Asserted
3	01/18/2000	13:59:00.880	RAISE	Deasserted
2	01/18/2000	13:59:08.613	VMINLMT	Asserted
1	01/18/2000	13:59:08.830	BLOCKSV	Asserted

=>

Figure 6.19: Test Scenario 3.7.2. Phase C Voltage Regulator SER

6.8.3 Voltage High- and Low-Limit Scenarios – No Operation

Table 6.7 describes the voltage regulator operation during a large system voltage increase or decrease.

Table 6.7: Voltage High- and Low-Limit Operations

Objective: Verify if the regulator determines whether voltage goes beyond the minimum and maximum voltage limits.					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. System with nominal voltage and current conditions: VA = 120 V ∠0° VB = 120 V ∠–120° VC = 120 V ∠+120° 2. Voltage regulator in AUTO and REMOTE modes. 3. Voltage regulation enabled. 4. Initial tap setting.	1. Lower test set voltage VA = 108 V ∠0° VB = 108 V ∠–120° VC = 108 V ∠+120°	1.a. **VOLTAGE LOW LIMIT** LED blinks red. 1.b. Tap operation does not initiate.	**VOLTAGE LOW LIMIT** LED blinks red when the voltage goes beyond the minimum lower limit. Tap operation does not initiate.	Y	
1. System with nominal voltage and current conditions: VA = 120 V ∠0° VB = 120 V ∠–120° VC = 120 V ∠+120° 2. Voltage regulator in AUTO and REMOTE modes. 3. Voltage regulation enabled. 4. Initial tap setting.	1. Raise test set voltage VA = 132 V ∠0° VB = 132 V ∠–120° VC = 132 V ∠+120°	1.a. **VOLTAGE HIGH LIMIT** LED blinks red. 1.b. Tap operation does not initiate.	**VOLTAGE HIGH LIMIT** LED blinks red when the voltage goes beyond the maximum higher limit. Tap operation does not initiate.	Y	
Test notes: Voltage regulator operation is verified for each phase. Observe that the switching operation does not take place.					

Figure 6.20 through Figure 6.25 illustrate voltage limit operations performed by the voltage regulators and their respective SER data. The test circuit was initially run at the normal operating load. The load was drastically increased after a certain time period, resulting in a large voltage drop in the system. The voltage regulators detected the voltage dipping below the voltage low limit and subsequently issued a BLOCKSV Relay Word bit to cease all tap operations. The time stamp with its voltage reading indicates the point at which this operation takes place.

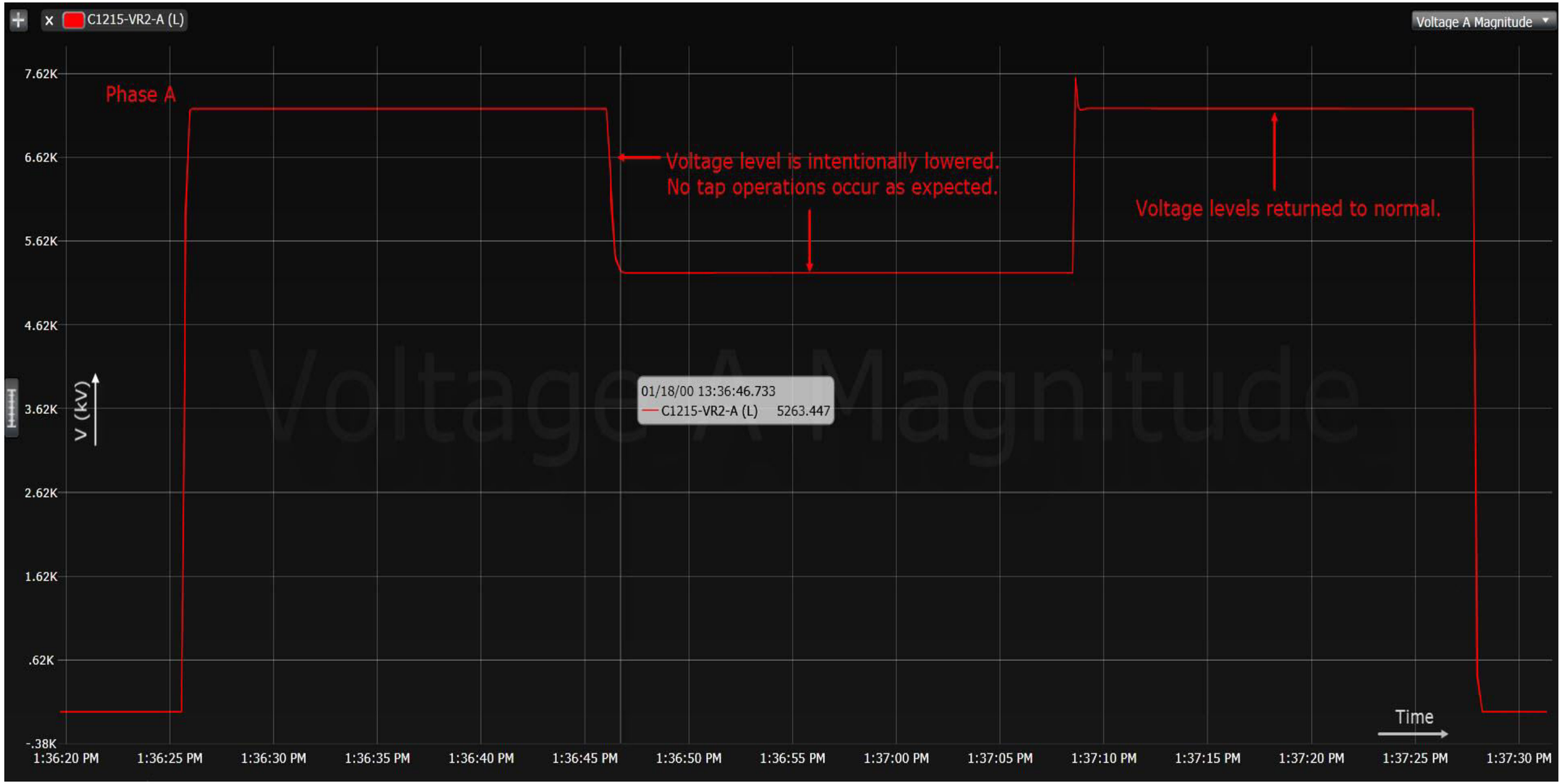
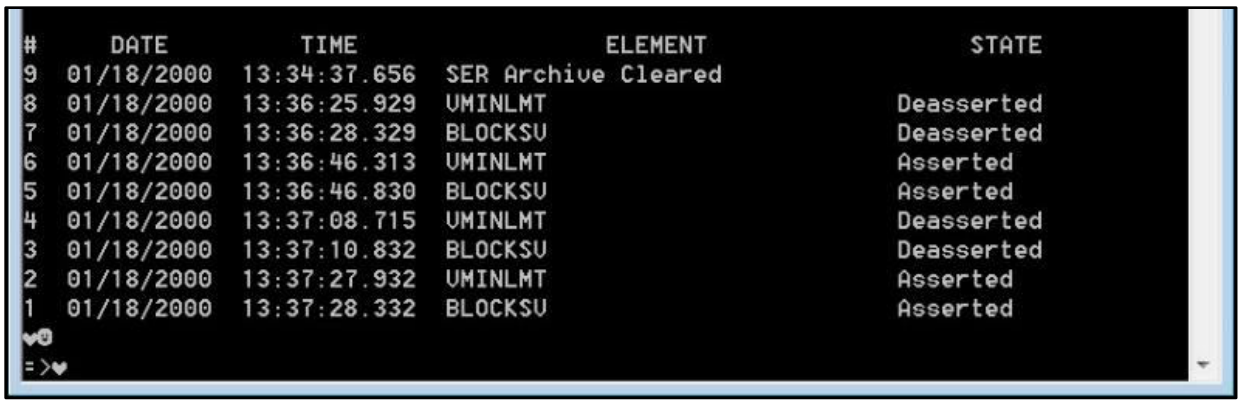


Figure 6.20: Test Scenario 3.7.3. Phase A Voltage Regulator Output Voltage Waveform



#	DATE	TIME	ELEMENT	STATE
9	01/18/2000	13:34:37.656	SER Archive Cleared	
8	01/18/2000	13:36:25.929	VMINLMT	Deasserted
7	01/18/2000	13:36:28.329	BLOCKSV	Deasserted
6	01/18/2000	13:36:46.313	VMINLMT	Asserted
5	01/18/2000	13:36:46.830	BLOCKSV	Asserted
4	01/18/2000	13:37:08.715	VMINLMT	Deasserted
3	01/18/2000	13:37:10.832	BLOCKSV	Deasserted
2	01/18/2000	13:37:27.932	VMINLMT	Asserted
1	01/18/2000	13:37:28.332	BLOCKSV	Asserted

=>

Figure 6.21: Test Scenario 3.7.3. Phase A Voltage Regulator SER

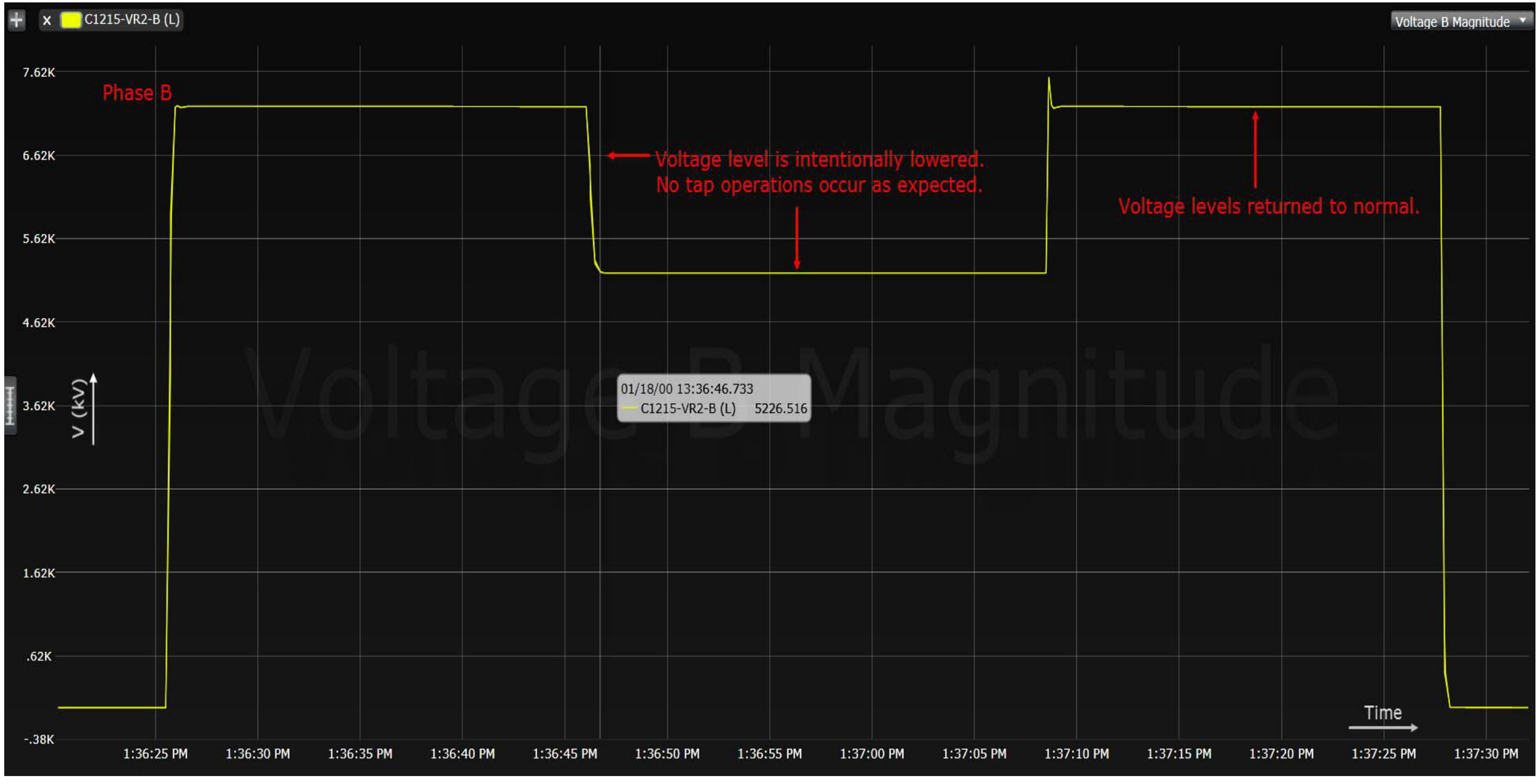
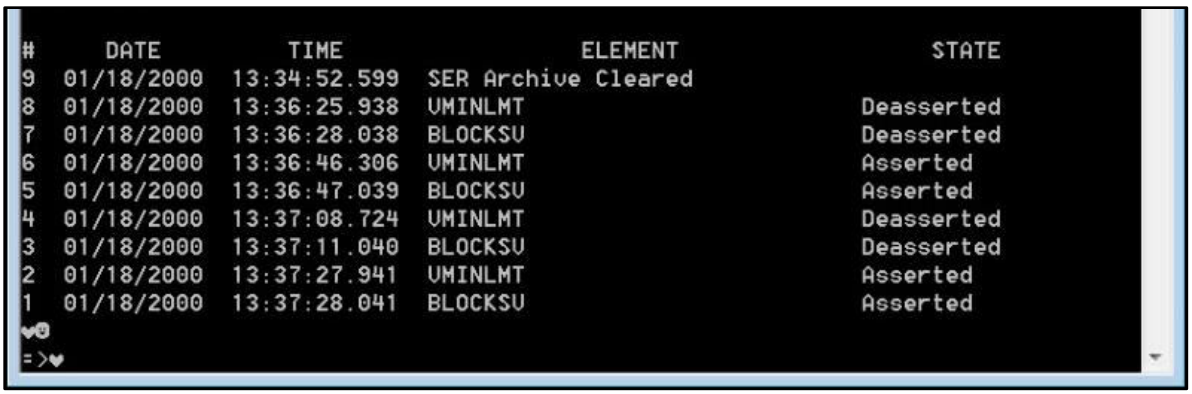


Figure 6.22: Test Scenario 3.7.3. Phase B Voltage Regulator Output Voltage Waveform

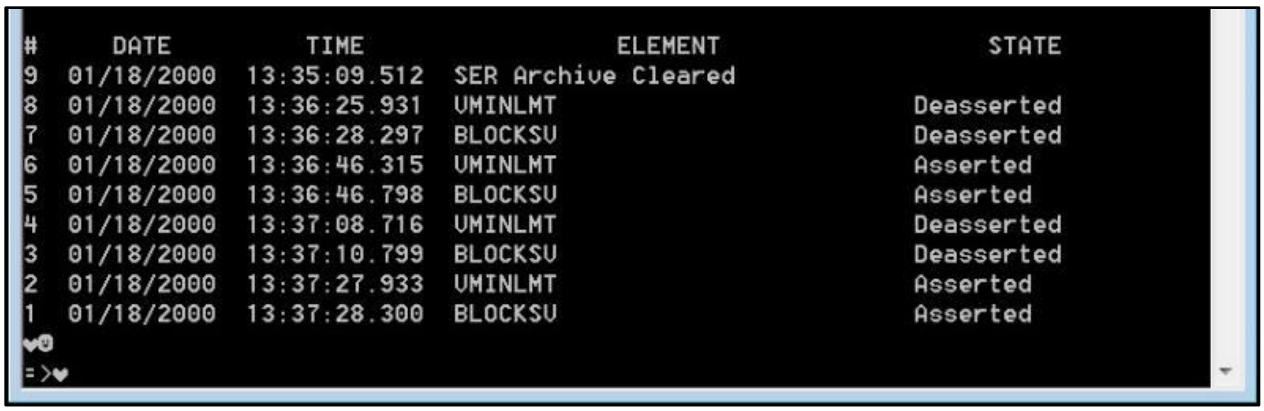


#	DATE	TIME	ELEMENT	STATE
9	01/18/2000	13:34:52.599	SER Archive Cleared	
8	01/18/2000	13:36:25.938	VMINLMT	Deasserted
7	01/18/2000	13:36:28.038	BLOCKSV	Deasserted
6	01/18/2000	13:36:46.306	VMINLMT	Asserted
5	01/18/2000	13:36:47.039	BLOCKSV	Asserted
4	01/18/2000	13:37:08.724	VMINLMT	Deasserted
3	01/18/2000	13:37:11.040	BLOCKSV	Deasserted
2	01/18/2000	13:37:27.941	VMINLMT	Asserted
1	01/18/2000	13:37:28.041	BLOCKSV	Asserted

=>

Figure 6.23: Test Scenario 3.7.3. Phase B Voltage Regulator SER

Figure 6.24: Test Scenario 3.7.3. Phase C Voltage Regulator Output Voltage Waveform



#	DATE	TIME	ELEMENT	STATE
9	01/18/2000	13:35:09.512	SER Archive Cleared	
8	01/18/2000	13:36:25.931	VMINLMT	Deasserted
7	01/18/2000	13:36:28.297	BLOCKSV	Deasserted
6	01/18/2000	13:36:46.315	VMINLMT	Asserted
5	01/18/2000	13:36:46.798	BLOCKSV	Asserted
4	01/18/2000	13:37:08.716	VMINLMT	Deasserted
3	01/18/2000	13:37:10.799	BLOCKSV	Deasserted
2	01/18/2000	13:37:27.933	VMINLMT	Asserted
1	01/18/2000	13:37:28.300	BLOCKSV	Asserted

=>

Figure 6.25: Test Scenario 3.7.3. Phase C Voltage Regulator SER

6.8.4 Load Profile Operation

Table 6.8 describes the operation of the voltage regulator during the 24-hour load profile run.

Table 6.8: Load Profile Operation

Objective: Verify the voltage regulator operation with the load profile enabled.					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. System with nominal voltage and current conditions: VA = 120 V ∠0° VB = 120 V ∠–120° VC = 120 V ∠+120° 2. Voltage regulator in AUTO and REMOTE modes. 3. Voltage regulation enabled. 4. Initial tap setting.	1. Run the RTDS model with the load scheduler ON.	1.a. **VOLTAGE LOW LIMIT** LED initially blinks red. 1.b. The voltage regulator detects the load voltage and raises or lowers the tap to bring the load voltage within the defined voltage band. 1.c. The above step repeats for each load step change.	1. The voltage regulator was observed to operate as desired, ensuring load voltage stayed within the defined voltage band for each load step.	Y	
Test notes: The voltage regulator operation is verified for each phase and for each load step change.					

The RTDS test case was run at the load profile provided by SDG&E and with a 2 V voltage regulation bandwidth. It was observed that the voltage regulators did not operate for the 24-hour load profile run. This was because the load variations do not lead to the system voltage crossing the forward bandwidth of the voltage regulators. This is illustrated for the Phase A voltage regulator in Figure 6.26 and Figure 6.27.

Based on recommendations from SDG&E, the load was increased considerably to best simulate the voltage regulator operation. The modified load profile was essentially the original load profile with each load point increased to three times the actual load. The modified load profile was run, resulting in voltage regulator operation. It was observed that the voltage regulators successfully regulated voltage at various points to bring the system voltage to within its normal operating band. Figure 6.28 through Figure 6.33 illustrate the voltage regulator operation with its corresponding SER data.

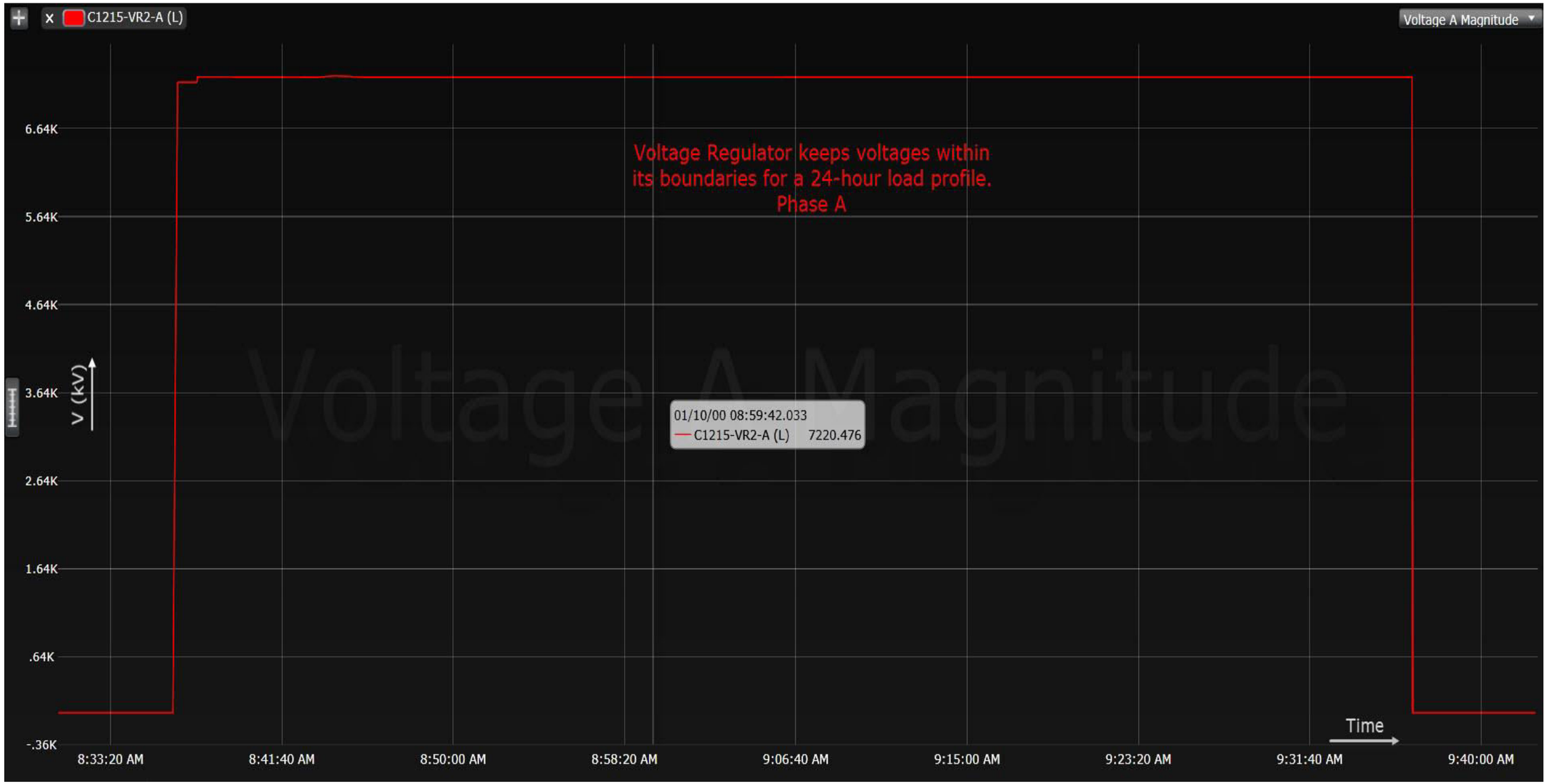
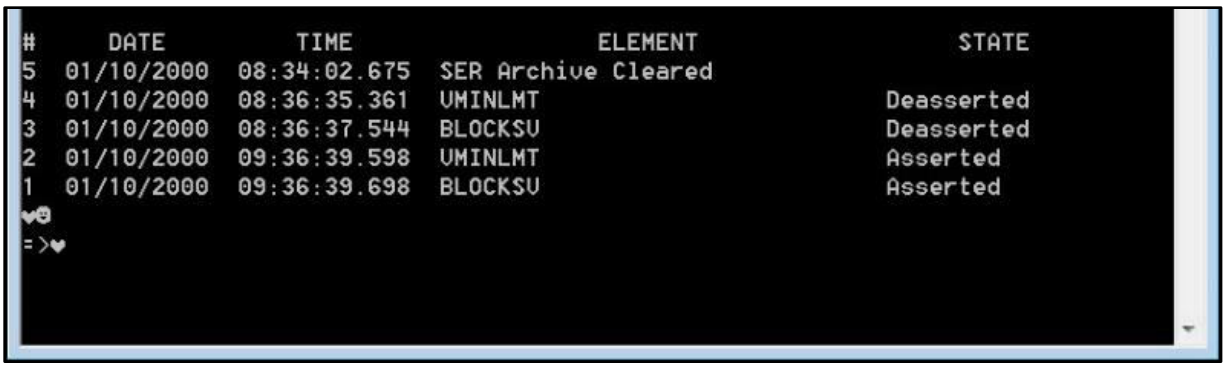


Figure 6.26: Test Scenario 3.7.4. Phase A Voltage Regulator Output Voltage Waveform – Normal Load Profile



#	DATE	TIME	ELEMENT	STATE
5	01/10/2000	08:34:02.675	SER Archive Cleared	
4	01/10/2000	08:36:35.361	VMINLMT	Deasserted
3	01/10/2000	08:36:37.544	BLOCK$V	Deasserted
2	01/10/2000	09:36:39.598	VMINLMT	Asserted
1	01/10/2000	09:36:39.698	BLOCK$V	Asserted

=>

Figure 6.27: Test Scenario 3.7.4. Phase A Voltage Regulator SER – Normal Load Profile

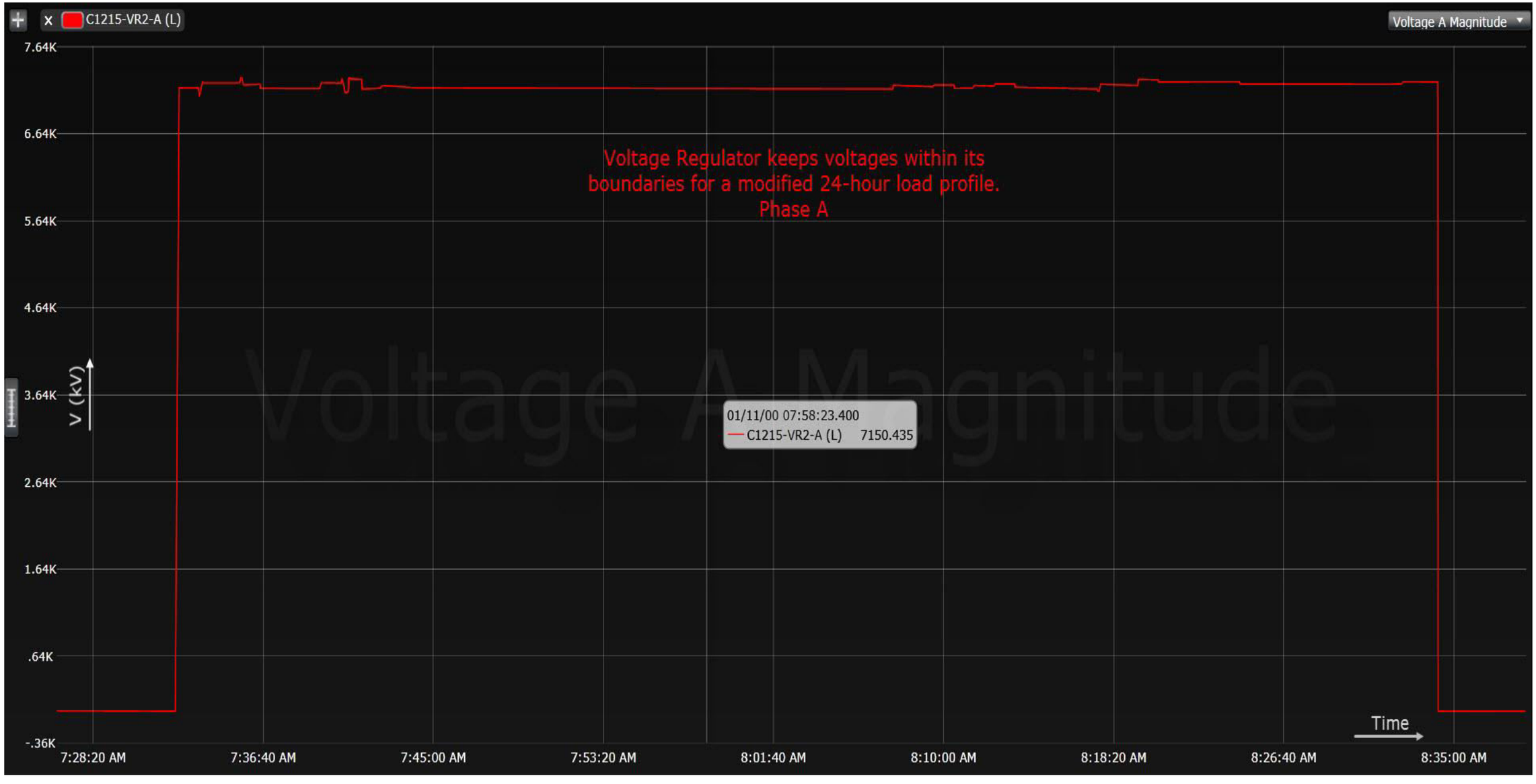
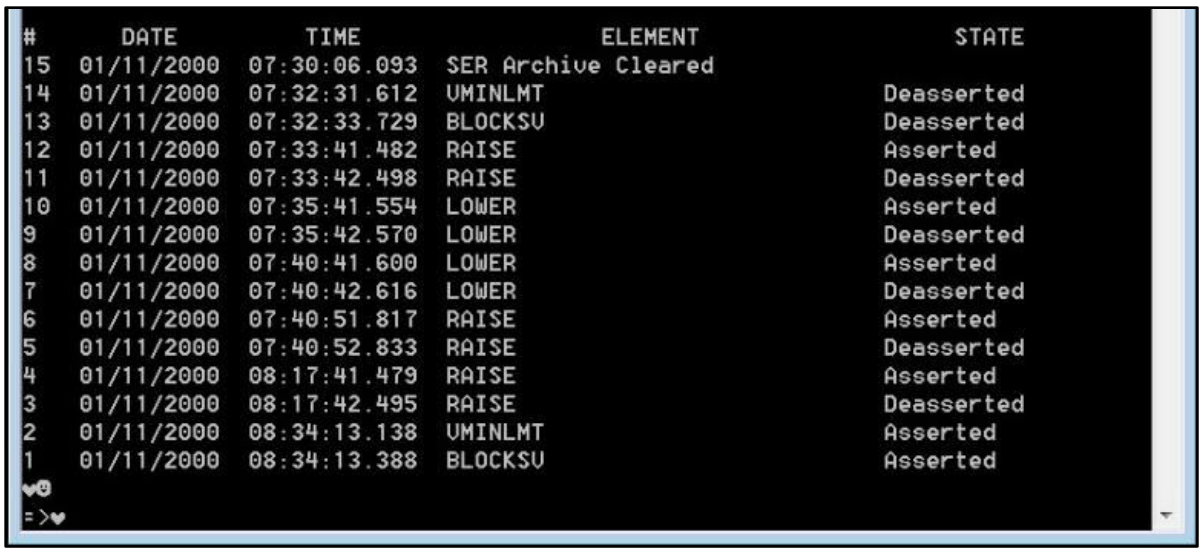


Figure 6.28: Test Scenario 3.7.4. Phase A Voltage Regulator Output Voltage Waveform – Modified Load Profile

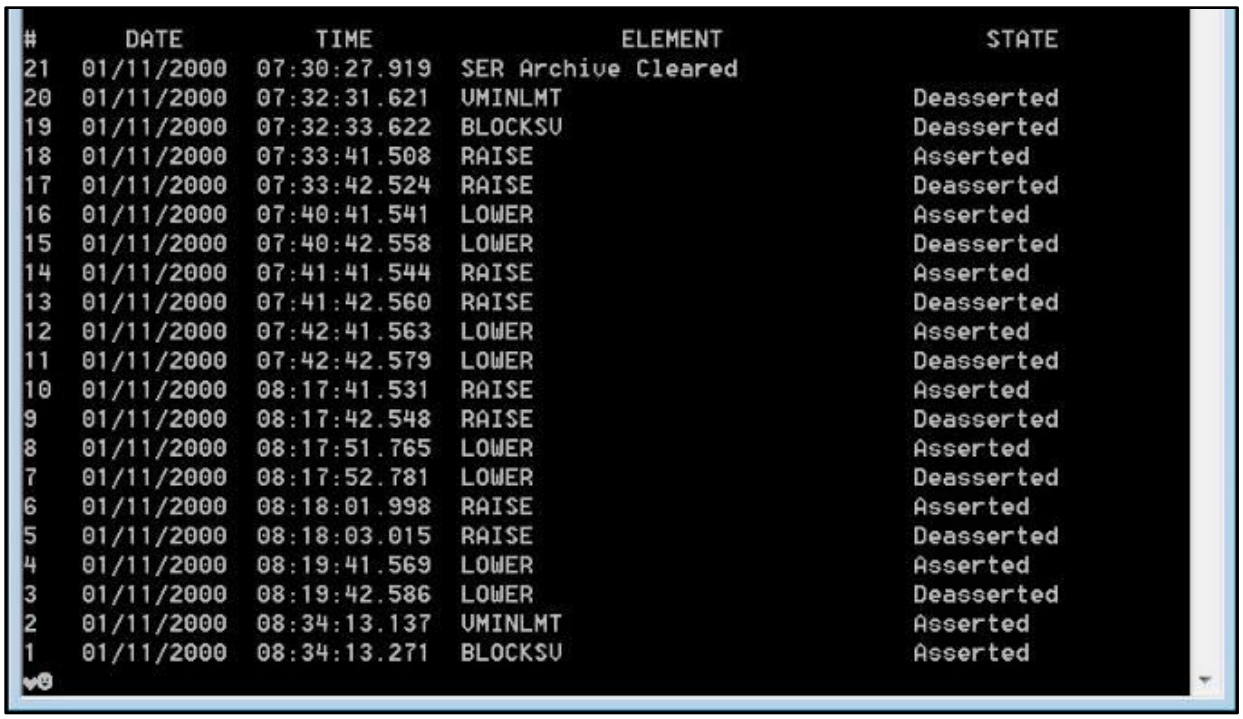


#	DATE	TIME	ELEMENT	STATE
15	01/11/2000	07:30:06.093	SER Archive Cleared	
14	01/11/2000	07:32:31.612	VMINLMT	Deasserted
13	01/11/2000	07:32:33.729	BLOCKSV	Deasserted
12	01/11/2000	07:33:41.482	RAISE	Asserted
11	01/11/2000	07:33:42.498	RAISE	Deasserted
10	01/11/2000	07:35:41.554	LOWER	Asserted
9	01/11/2000	07:35:42.570	LOWER	Deasserted
8	01/11/2000	07:40:41.600	LOWER	Asserted
7	01/11/2000	07:40:42.616	LOWER	Deasserted
6	01/11/2000	07:40:51.817	RAISE	Asserted
5	01/11/2000	07:40:52.833	RAISE	Deasserted
4	01/11/2000	08:17:41.479	RAISE	Asserted
3	01/11/2000	08:17:42.495	RAISE	Deasserted
2	01/11/2000	08:34:13.138	VMINLMT	Asserted
1	01/11/2000	08:34:13.388	BLOCKSV	Asserted

=>

Figure 6.29: Test Scenario 3.7.4. Phase A Voltage Regulator SER – Modified Load Profile

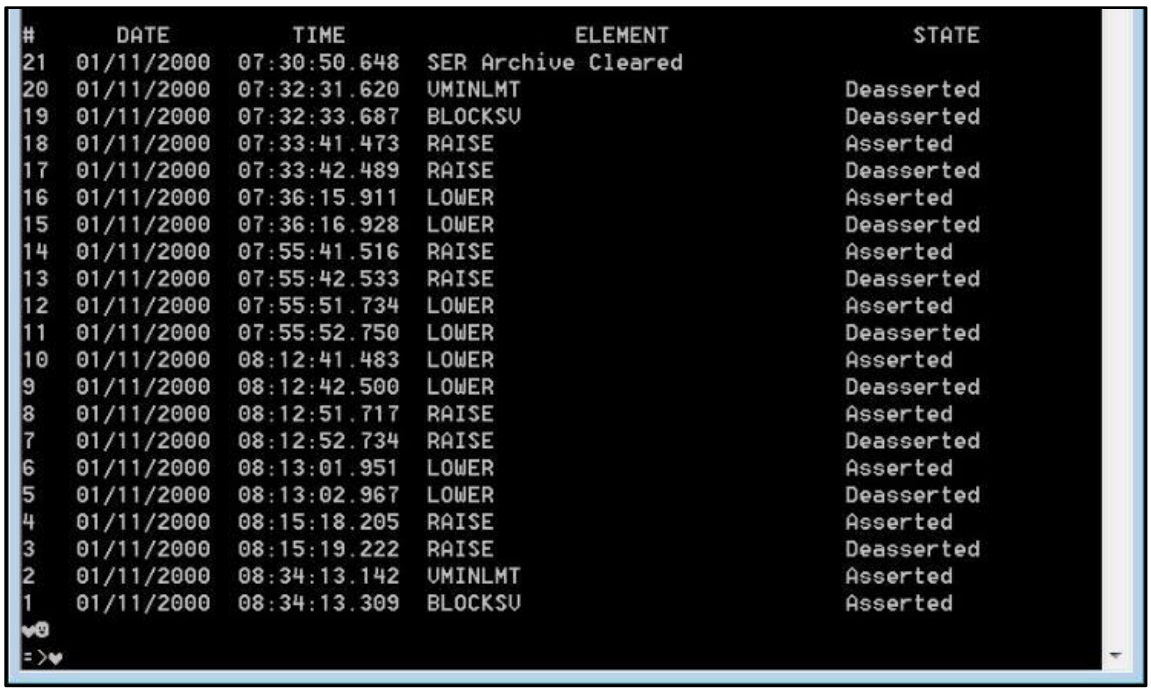
Figure 6.30: Test Scenario 3.7.4. Phase B Voltage Regulator Output Voltage Waveform – Modified Load Profile



#	DATE	TIME	ELEMENT	STATE
21	01/11/2000	07:30:27.919	SER Archive Cleared	
20	01/11/2000	07:32:31.621	VMINLMT	Deasserted
19	01/11/2000	07:32:33.622	BLOCKSV	Deasserted
18	01/11/2000	07:33:41.508	RAISE	Asserted
17	01/11/2000	07:33:42.524	RAISE	Deasserted
16	01/11/2000	07:40:41.541	LOWER	Asserted
15	01/11/2000	07:40:42.558	LOWER	Deasserted
14	01/11/2000	07:41:41.544	RAISE	Asserted
13	01/11/2000	07:41:42.560	RAISE	Deasserted
12	01/11/2000	07:42:41.563	LOWER	Asserted
11	01/11/2000	07:42:42.579	LOWER	Deasserted
10	01/11/2000	08:17:41.531	RAISE	Asserted
9	01/11/2000	08:17:42.548	RAISE	Deasserted
8	01/11/2000	08:17:51.765	LOWER	Asserted
7	01/11/2000	08:17:52.781	LOWER	Deasserted
6	01/11/2000	08:18:01.998	RAISE	Asserted
5	01/11/2000	08:18:03.015	RAISE	Deasserted
4	01/11/2000	08:19:41.569	LOWER	Asserted
3	01/11/2000	08:19:42.586	LOWER	Deasserted
2	01/11/2000	08:34:13.137	VMINLMT	Asserted
1	01/11/2000	08:34:13.271	BLOCKSV	Asserted

Figure 6.31: Test Scenario 3.7.4. Phase B Voltage Regulator SER – Modified Load Profile

Figure 6.32: Test Scenario 3.7.4. Phase C Voltage Regulator Output Voltage Waveform – Modified Load Profile



#	DATE	TIME	ELEMENT	STATE
21	01/11/2000	07:30:50.648	SER Archive Cleared	
20	01/11/2000	07:32:31.620	VMINLMT	Deasserted
19	01/11/2000	07:32:33.687	BLOCKSV	Deasserted
18	01/11/2000	07:33:41.473	RAISE	Asserted
17	01/11/2000	07:33:42.489	RAISE	Deasserted
16	01/11/2000	07:36:15.911	LOWER	Asserted
15	01/11/2000	07:36:16.928	LOWER	Deasserted
14	01/11/2000	07:55:41.516	RAISE	Asserted
13	01/11/2000	07:55:42.533	RAISE	Deasserted
12	01/11/2000	07:55:51.734	LOWER	Asserted
11	01/11/2000	07:55:52.750	LOWER	Deasserted
10	01/11/2000	08:12:41.483	LOWER	Asserted
9	01/11/2000	08:12:42.500	LOWER	Deasserted
8	01/11/2000	08:12:51.717	RAISE	Asserted
7	01/11/2000	08:12:52.734	RAISE	Deasserted
6	01/11/2000	08:13:01.951	LOWER	Asserted
5	01/11/2000	08:13:02.967	LOWER	Deasserted
4	01/11/2000	08:15:18.205	RAISE	Asserted
3	01/11/2000	08:15:19.222	RAISE	Deasserted
2	01/11/2000	08:34:13.142	VMINLMT	Asserted
1	01/11/2000	08:34:13.309	BLOCKSV	Asserted

=>

Figure 6.33: Test Scenario 3.7.4. Phase C Voltage Regulator SER – Modified Load Profile

6.9 RECOMMENDATIONS

The recommended standard for voltage regulation as specified by SDG&E was ±5 percent, which equates to a forward bandwidth of 12 V. However, it is recommended to narrow the forward bandwidth to 2 V to allow for a better regulation. This would ensure less fluctuations in the regulated voltage and steady control over the standard voltage limits.

7 CAPACITOR BANK CONTROLLER

This section demonstrates the functions and capabilities of a capacitor bank controller. The capacitor bank controller continuously monitors the circuit parameters and switches in and out based on set criteria. The analysis and understanding of the capacitor bank controller, as a stand-alone device for correcting the voltage profile, is helpful in enhancing the voltage support coordination scheme using multiple devices described in Section 10.

This section provides the test procedure to demonstrate the various modes of operation including time of day (TOD), voltage, and KVAR for a CBC on a distribution circuit. It also provides test procedures for protection lockout functionalities. For this test, LOCAL/SUPY (supervisory) and AUTO/MANUAL modes of operation are considered. Results are recorded at the end of each test.

Tests are carried out to evaluate the best times to switch the capacitor bank in or out, based on the load and voltage profile of the modeled SDG&E test circuits.

The choice of controller does not affect the type of tests. The controller controls capacitor 131CW in the coastal-residential test circuit. The power quality meter, located downstream of 131CW at Bus P322964, is considered as a line monitor on the circuit. Refer to Appendix A for the one-line diagram of the test circuit. The coastal-residential test circuit has two capacitors: a 131CW (SCADA capacitor) and a 461CW (fixed capacitor).

7.1 TEST SETUP

This section includes details on the hardware test setup assembly in the laboratory environment.

7.1.1 I/O List

Table 7.1 shows the designated I/O contacts for the controller. The 52b contacts are used to indicate the switch status.

Table 7.1: Controller I/O List

Output Contact	Function	Input Contact	Function
OUT101	Open Phase A	IN102	52b Phase A
OUT301	Open Phase B	IN302	52b Phase B
OUT303	Open Phase C	IN304	52b Phase C
OUT102	Close Phase A	–	–
OUT302	Close Phase B	–	–
OUT304	Close Phase C	–	–

7.1.2 Front-Panel Layout

Figure 7.1 illustrates the proposed front-panel layout of the controller. The selected controller has 8 operator-controlled pushbuttons and 22 programmable LEDs.

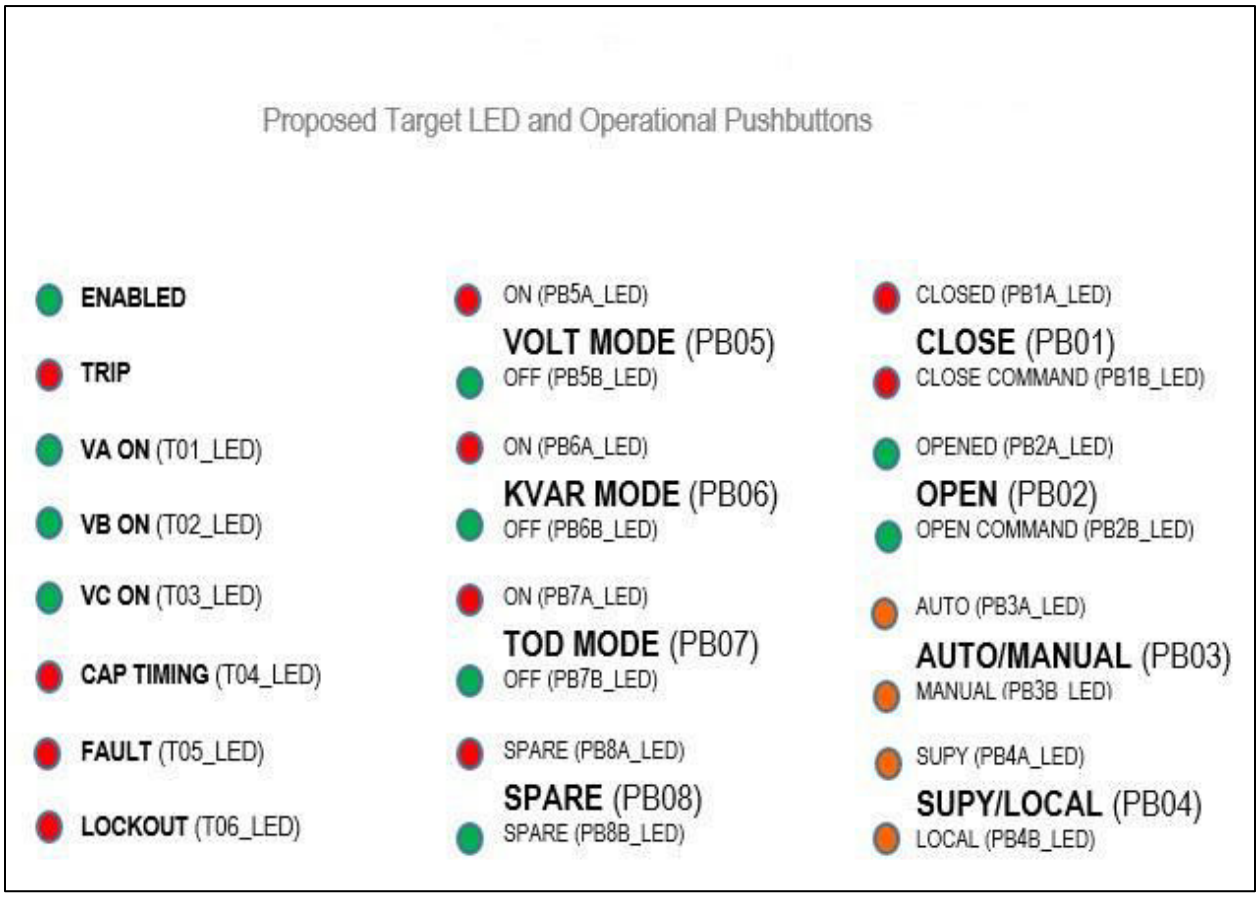


Figure 7.1: Controller Front-Panel Layout

7.1.3 Low-Level Test Interface

The controller has a low-level test interface on the four ACI/AVI current/voltage cards with both low-level voltage inputs and regular voltage inputs in Slot Z as shown in Figure 7.2. The RTDS analog outputs channel is connected to the controller via Connector J2 on Slot Z card with a ribbon cable.

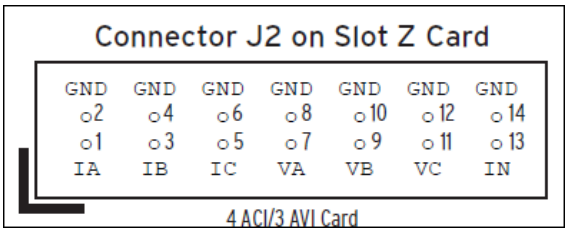


Figure 7.2: Controller Low-Level Test Interface J2

7.1.4 RTDS and Relay Interface

Figure 7.3 illustrates the interface between the RTDS and the controller/power quality meter. The controller is connected to the RTDS I/O cube such that it receives analog and digital inputs from the RTDS, and sends digital outputs or control signals to the RTDS. The power quality meter is connected to receive analog inputs from the RTDS.

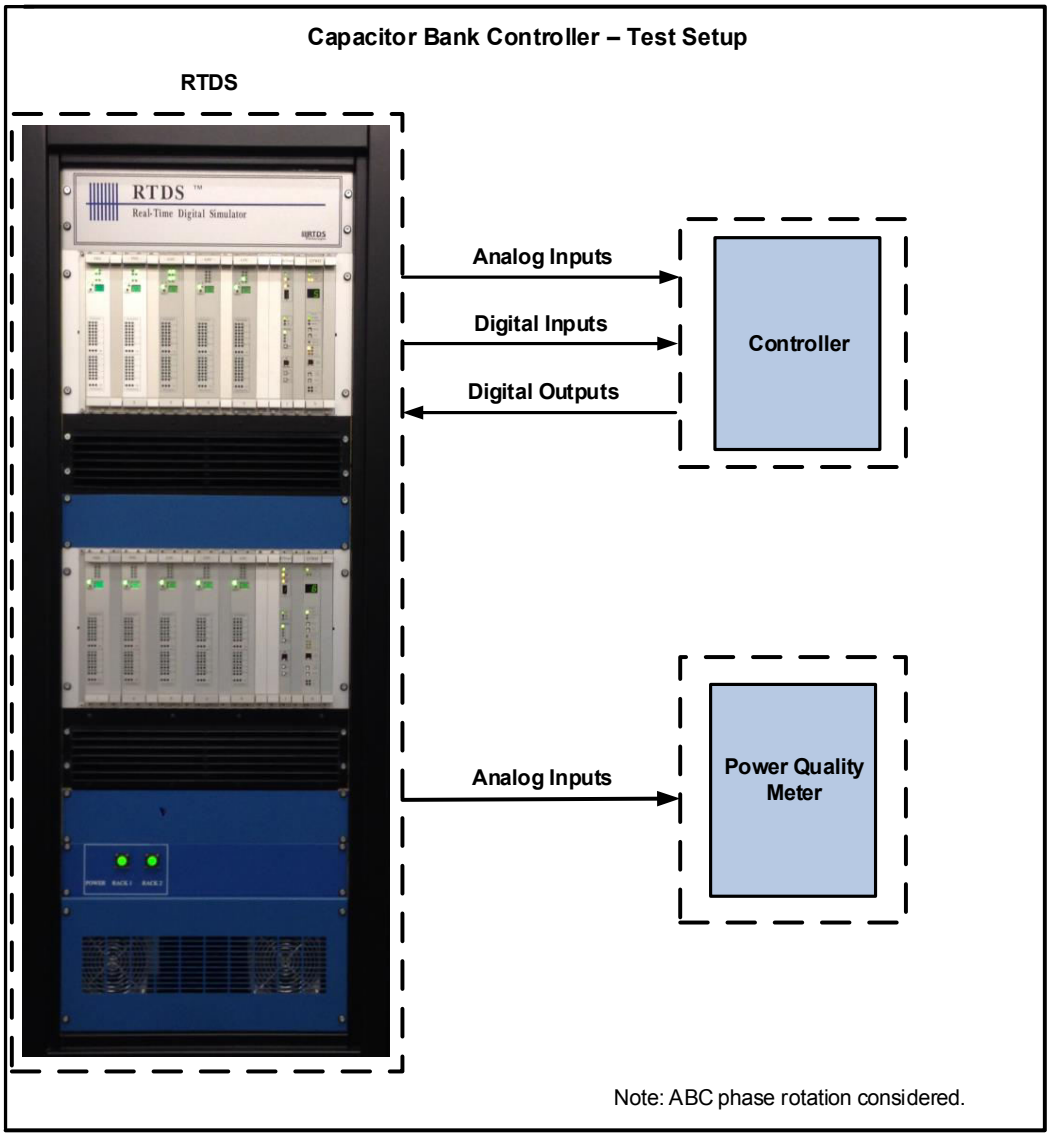


Figure 7.3: CBC – Test Setup

Figure 7.4 illustrates analog inputs from the RTDS to the controller and the power quality meter via the GTAO Cards 3 and 4, respectively.

- GTAO Card 3: Channels 7 through 9 are reserved for currents and Channels 10 through 12 are reserved for line-to-neutral voltages for the controller.
- GTAO Card 4: Channels 7 through 9 are reserved for line-to-neutral voltages for the power quality meter.

Figure 7.5 and Figure 7.6 show the mapping for digital inputs and digital outputs, respectively, via the GTFPI card.

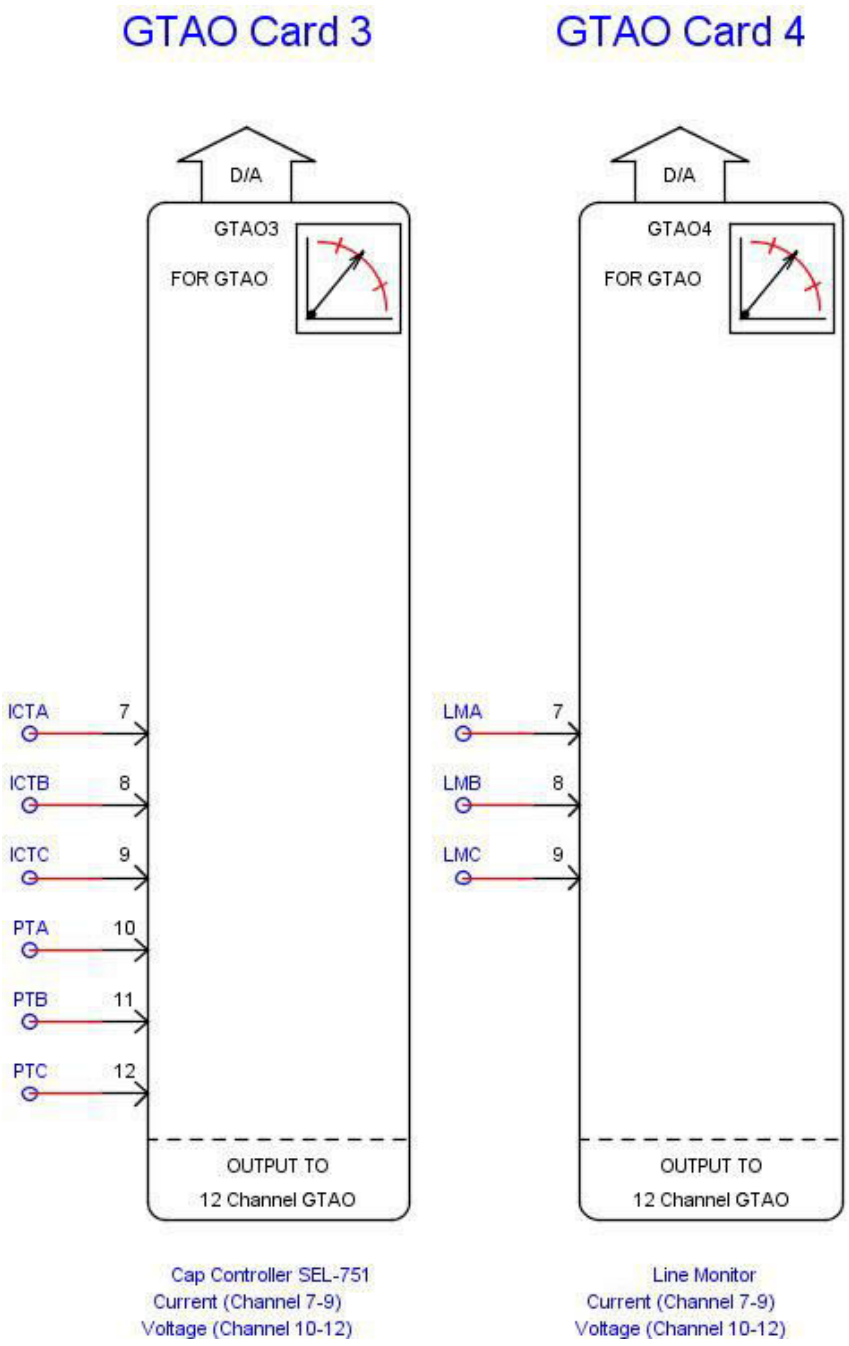


Figure 7.4: RTDS and Controller Interface – Analog Inputs

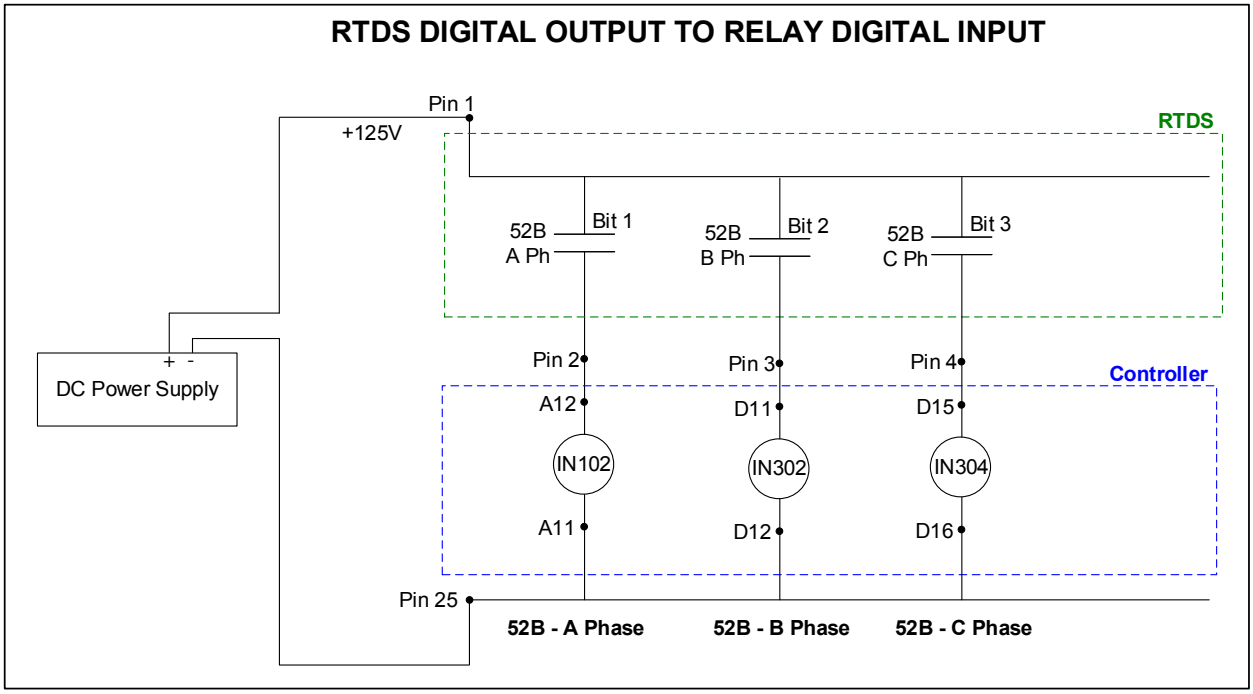


Figure 7.5: RTDS and Controller Interface – Digital Inputs

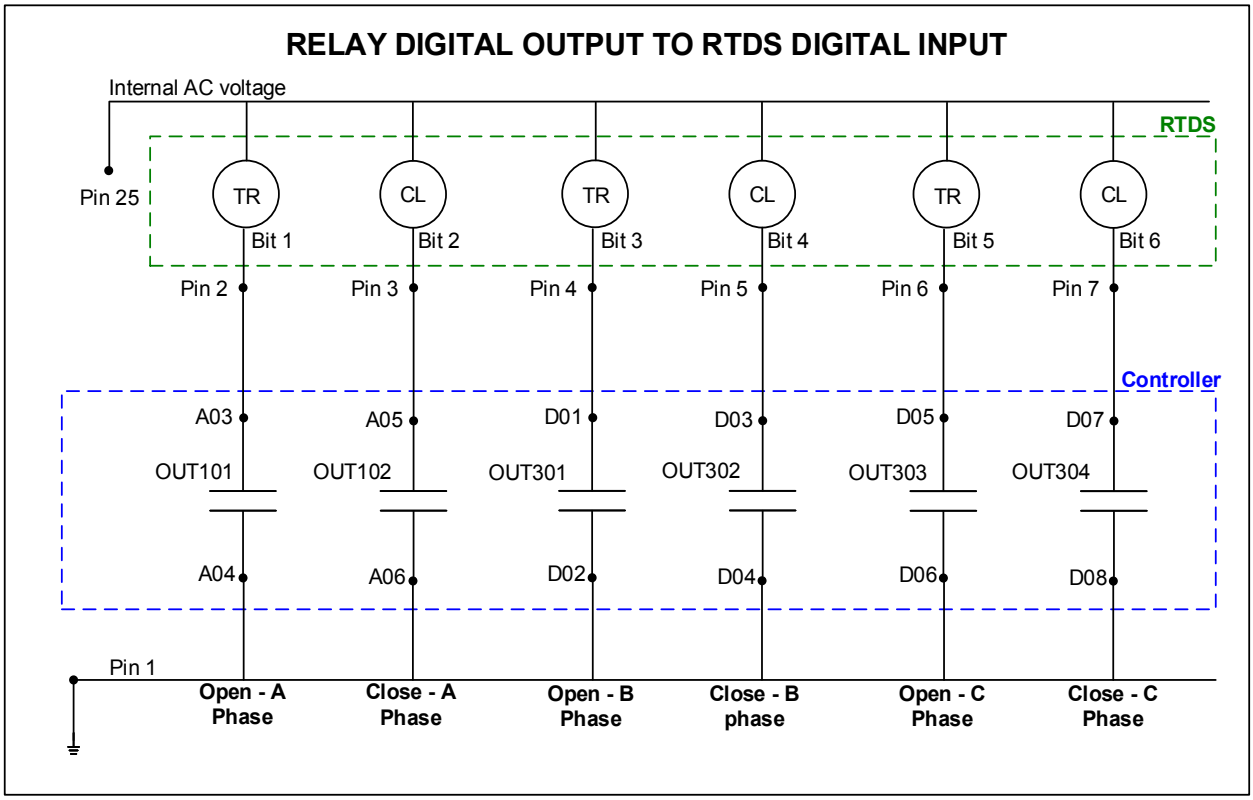


Figure 7.6: RTDS and Controller Interface – Digital Outputs

7.1.5 Tests Summary

The following tests were performed by the capacitor bank controller:

1. Modes of operations

    a. SUPY/LOCAL: SUPY refers to supervisory or remote control via SCADA. LOCAL mode refers to control via the relay front panel.

    b. AUTO/ MANUAL: AUTO refers to automatic control via various control strategies defined in the relay logic. MANUAL mode disables automatic switching operations.

    Capacitor bank switching can be carried out via:

        i. Pushbuttons when the controller is in LOCAL and MANUAL modes.

        ii. SCADA controls when the controller is in SUPY and MANUAL modes.

        iii. Voltage, KVAR, and TOD modes when the controller is in LOCAL and AUTO modes.

2. Automatic control strategies

    a. Voltage control

    When AUTO and Voltage Control modes are enabled and rms line-to-neutral voltage on all the phases is above the high-voltage threshold or below the low-voltage threshold, the controller starts timing to open or close the capacitor bank breaker. During this time, the front-panel LEDs indicate pending open or close operation. If the condition persists for 1 second (user settable), the controller initiates the capacitor bank switching.

    Voltage conditions out of the normal operating band are simulated. The voltage profile is observed post-capacitor bank switching.

    b. KVAR control

    When AUTO and KVAR Control modes are enabled, the controller operates the capacitor bank based on the measured reactive power load. Active power flow must be in the forward direction.

    When the lagging or leading reactive power exceeds the respective threshold, the controller will begin timing to operate. Refer Figure 7.7. During this time, the front-panel LEDs indicate the pending operation. If the condition persists for 1 second (user settable), the controller initiates the capacitor bank switching.

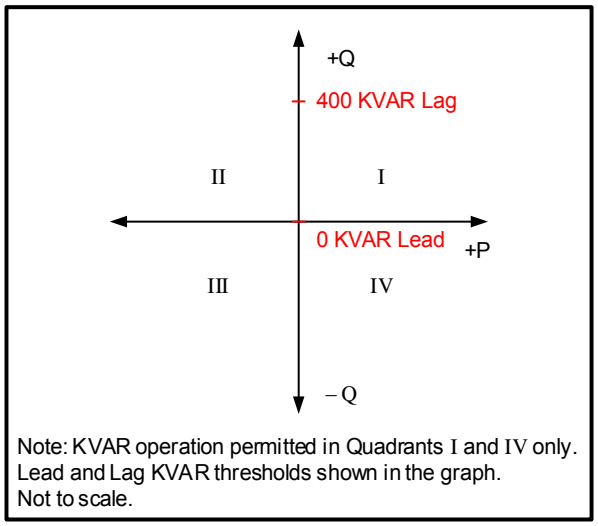


Figure 7.7: CBC KVAR Operations – Quadrants I and IV

c. TOD control

The controller provides two TOD programs: one for weekdays and one for weekends, which open and close the capacitor bank breaker based on the time of day. The controller initiates a close when the time reaches the close time setting and opens when the time reaches the open time setting.

Based on the testing carried out on the modeled SDG&E circuits, the best TOD operation setting will be evaluated.

3. Protection lockouts/alarms

a. Overvoltage lockout

If the measured voltage increases above the set threshold, the controller opens the switch and latches a lockout indication. This condition can be reset locally or remotely.

b. Voltage imbalance lockout

If the calculated voltage imbalance increases the set threshold, the controller opens the switch and latches a lockout indication. This condition can be reset locally or remotely.

c. High-current alarm

If the system current exceeds the set threshold, the controller alarms for as long as the high-current condition is present. The front-panel LED is programmed for this alarm. A high-current alarm condition does not inhibit any switching operations. It is understood that the upstream protection will arrest the high-current condition in the system.

4. Hunting lockout

The controller activates the hunting process any time the capacitor bank switch opens or closes while in AUTO mode. It remains active for the time set by the hunting time window setting. The controller counts each successive open and close operation while in AUTO mode.

When the hunting processing is active, a timer counts the minutes elapsed from the first switching operation. If the number of operations reaches the maximum allowed count, the controller latches in a hunting lockout. All automatic control ceases when a hunting lockout is latched in.

A hunting lockout latch can be reset remotely or locally.

5. Operations counter for SCADA

   The controller is programmed to count the number of open/close operations based on the following time periods. This information can be passed on to SCADA via DNP3 as analog inputs and can be used for further operational analysis.

   a. Since installation

   b. Yearly

   c. Daily

7.1.6 Analog Thresholds

Table 7.2 illustrates the thresholds used in these tests.

Table 7.2: Capacitor Bank Controller Analog Thresholds

SR. NO.	Primary	Secondary	Notes
Nominal voltage (L-N)	6.9 kV	69 V	Circuit specification
Capacitor bank size (single phase [1-ph])	400 KVAR	–	Circuit specification
PT ratio	100	–	–
CT ratio	600	–	–
Low-voltage threshold	6.55 kV	65.55 V	–5% of nominal
High-voltage threshold	7.24 kV	72.45 V	+5% of nominal
Lagging KVAR threshold (1-ph)	400 KVAR	6.67 VAR	–
Leading KVAR threshold (1-ph)	0 KVAR	0 VAR	–
Voltage imbalance threshold	–	–	3%
Overvoltage threshold	7.6 kV	76 V	+10% of nominal
High-current threshold	600 A	1 A	600 A
Hunting time window	–	–	60 min
Hunting count threshold	–	–	5 counts
TOD1 start day	–	–	2
TOD1 stop day	–	–	6
TOD1 close time	–	–	930 min (15:30:00)
TOD1 open time	–	–	300 min (05:00:00)
TOD2 start day	–	–	7
TOD2 stop day	–	–	1
TOD2 close time	–	–	930 min (15:30:00)
TOD2 open time	–	–	300 min (05:00:00)

7.2 TEST SCENARIOS AND RESULTS

Figure 7.8 is divided into three horizontal screens. The first screen shows the status of the capacitor bank controller operating modes – enabled or disabled. The second tab shows if any lockout conditions are present. The third tab shows the status of the capacitor bank breaker. If 52B is asserted, the breakers are opened, and if 52B is de-asserted, the breakers are closed. The top right-side shows "digital"- this implies that the screenshot refers to the digital results for the test under discussion. This layout is applicable to all digital test results capture in this section.

7.2.1 SUPY and LOCAL Toggle

Table 7.3: SUPY and LOCAL Toggle

Objective: Verify appropriate indication for SUPY/LOCAL operating mode.					
Specific instruction: Carry out Test Action 1, observe corresponding results. Move on to Test Action 2.					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. Controller in LOCAL mode. **LOCAL** LED is ON.	1. Press PB04. 2. Press PB04.	1.a. **SUPY** LED – ON 1.b. **LOCAL** LED – OFF 1.c. Controller in SUPY mode 2.a. **SUPY** LED – OFF 2.b. **LOCAL** LED – ON 2.c. Controller in LOCAL mode	Refer to Figure 7.8 and Figure 7.9.	Y	
Test notes: SUPY/LOCAL toggle allowed in either AUTO or MANUAL mode.					

Results/observations: Figure 7.8 shows SUPY mode is enabled because of Test Action 1 shown in Table 7.3. Figure 7.9 shows SUPY mode is disabled, which implies that LOCAL mode is enabled because of Test Action 2 shown in Table 7.3. Accurate observations were made on the relay front-panel LED.

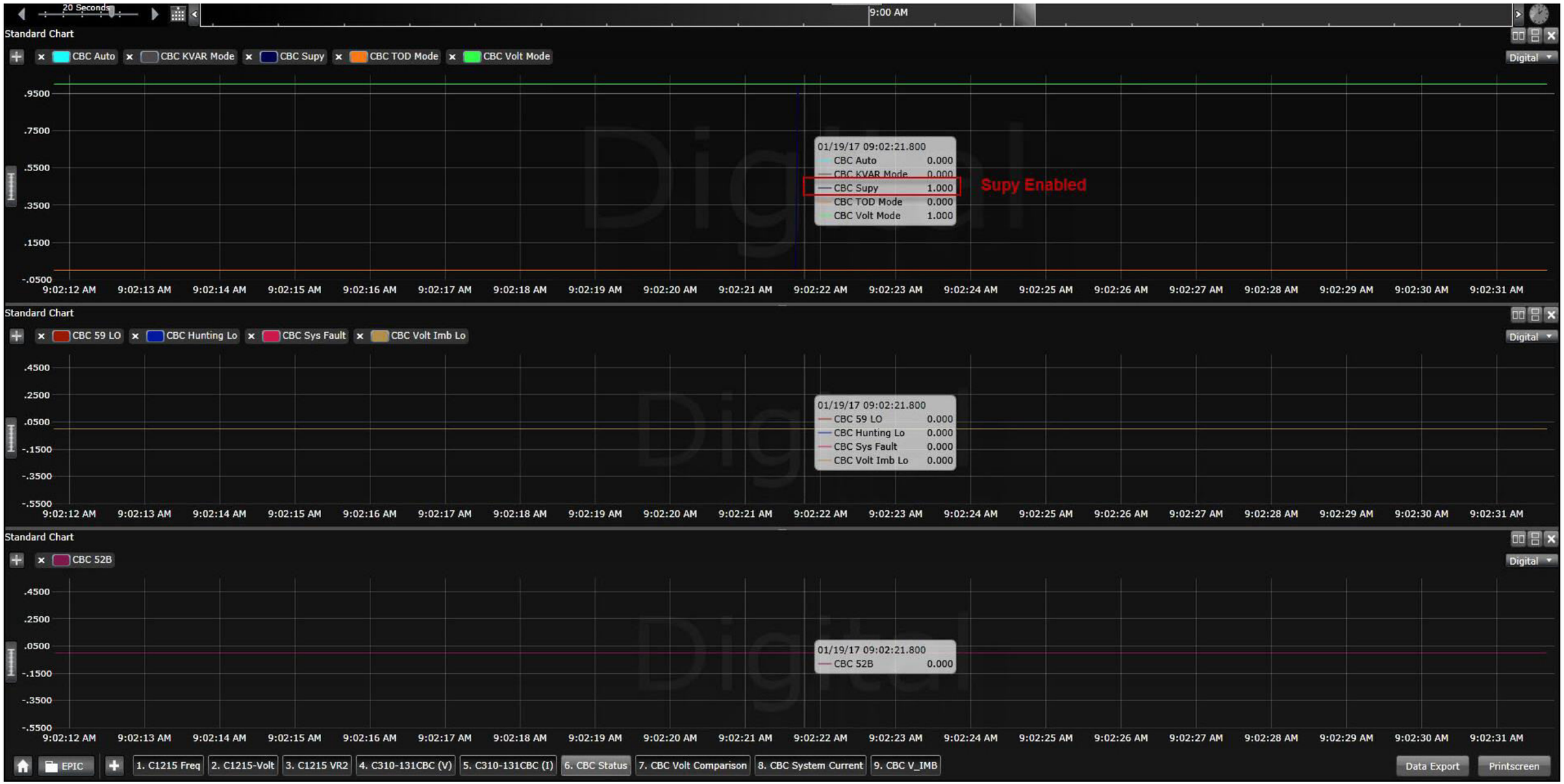


Figure 7.8: CBC SUPY Mode Enabled

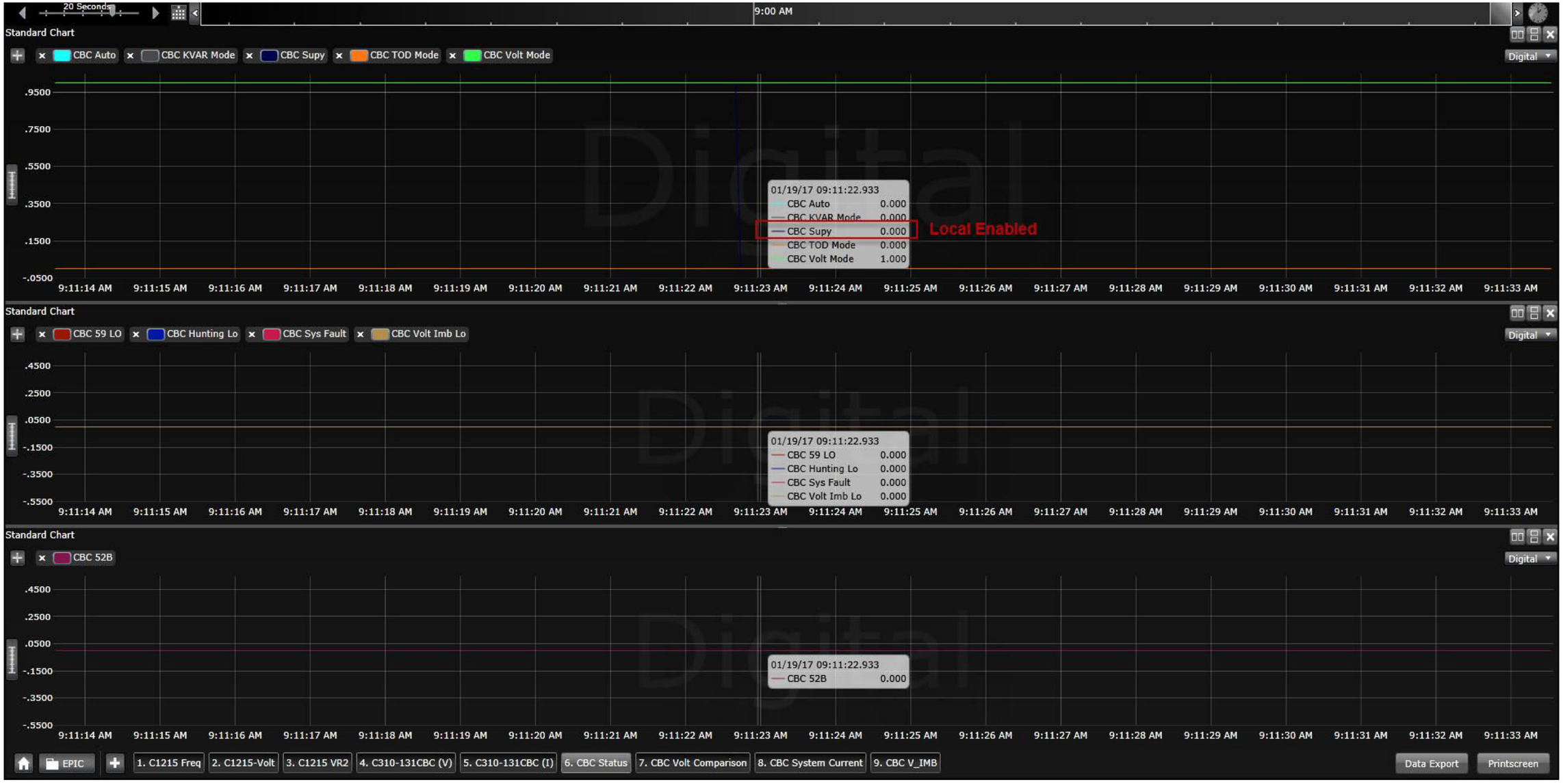


Figure 7.9: CBC LOCAL Mode Enabled

7.2.2 AUTO and MANUAL Toggle – From LOCAL Control

Table 7.4: AUTO and MANUAL Toggle – LOCAL Control

Objective: Verify appropriate indication for AUTO/MANUAL operating mode.					
Specific instruction: AUTO/MANUAL toggle allowed by PB03 in LOCAL mode. Carry out Test Action 1, observe corresponding results. Move on to Test Action 2.					
Negative test: Verify modes do not toggle via remote bits when in LOCAL.					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. Controller in MANUAL mode. **MANUAL** LED is ON.	1. Press PB03. 2. Press PB03.	1.a. **AUTO** LED – ON 1.b. **MANUAL** LED – OFF 1.c. Controller in AUTO mode 2.a. **AUTO** LED – OFF 2.b. **MANUAL** LED – ON 2.c. Controller in MANUAL mode	Refer to Figure 7.10 and Figure 7.11.	Y	
Test notes: The controller may be placed in AUTO mode when there are no lockout conditions and all three-phase voltages are healthy.					

Results/observations: Figure 7.10 shows AUTO mode is enabled because of Test Action 1 shown in Table 7.4. Figure 7.11 shows AUTO mode is disabled, which implies that MANUAL mode is enabled because of Test Action 2 shown in Table 7.4. Accurate observations were made on the relay front-panel LED.

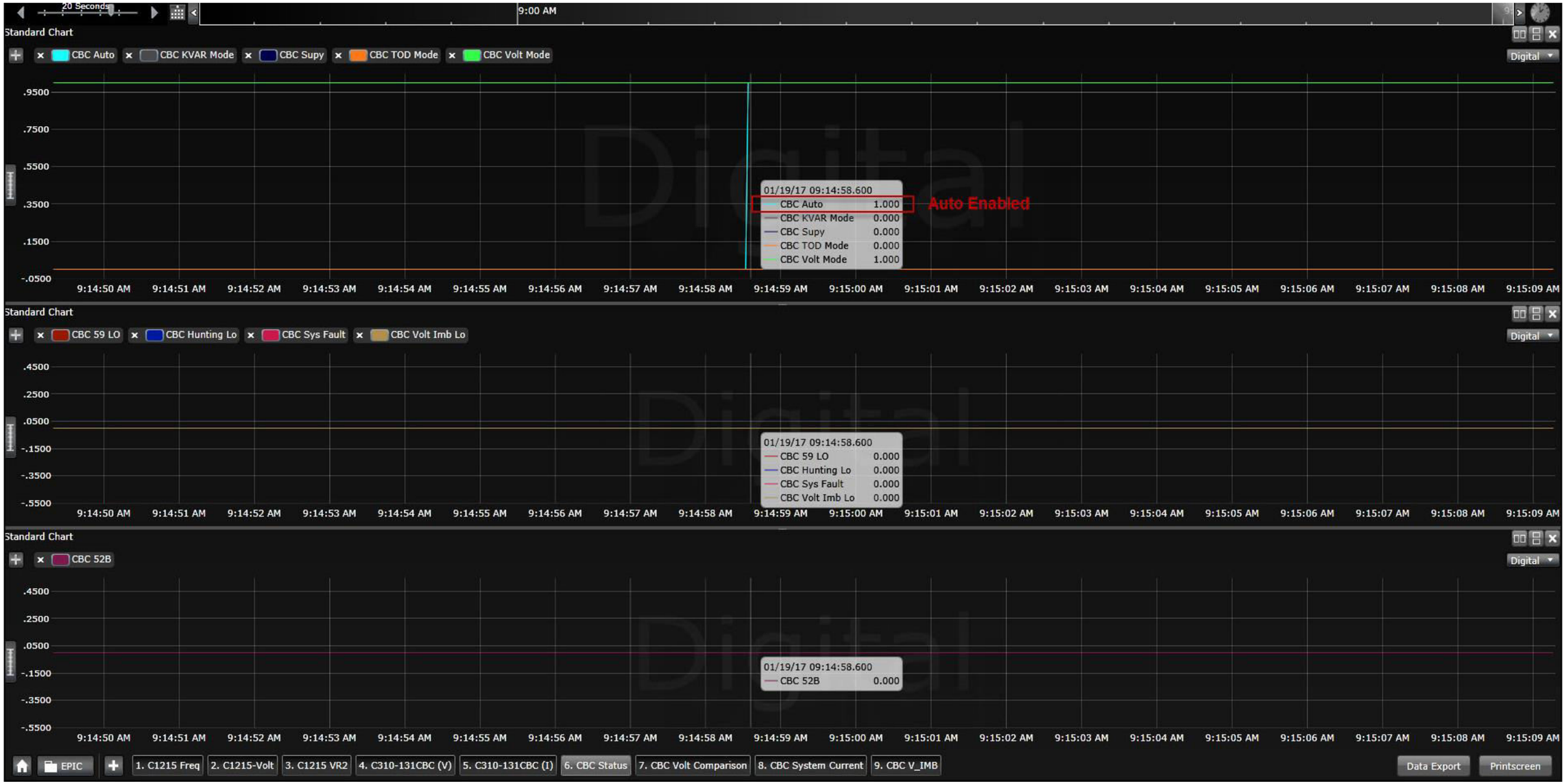


Figure 7.10: CBC AUTO Mode Enabled

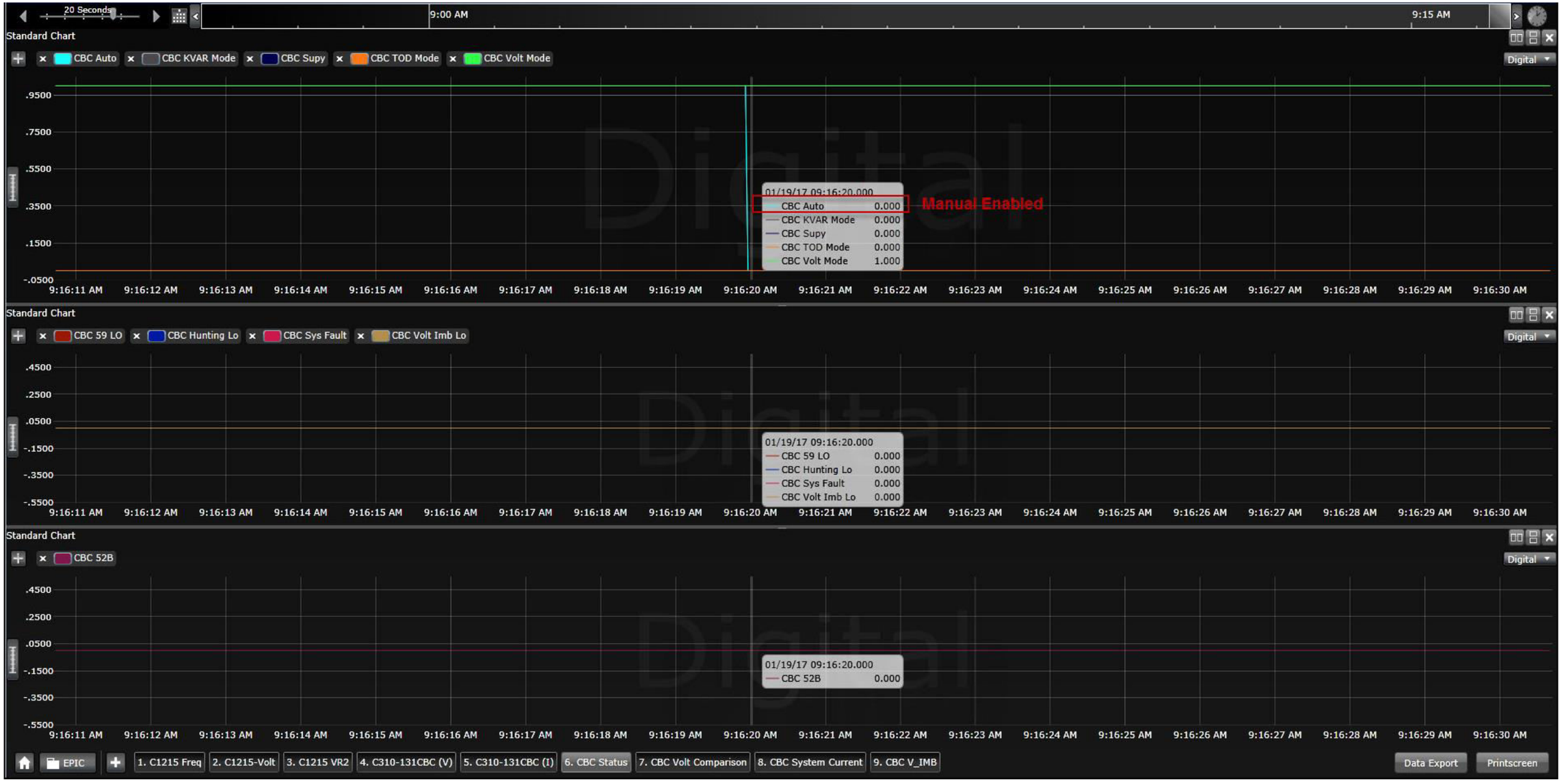


Figure 7.11: CBC MANUAL Mode Enabled

7.2.3 Automatic Voltage Control Operation

When the controller is set to AUTO mode while Voltage control mode is enabled via PB05, the controller automatically opens and closes the capacitor bank to maintain the voltage between the high-voltage threshold and the low-voltage threshold. **Line-to-neutral voltages for all three phases must be outside the thresholds for valid operations.** Refer to Table 7.5 and Table 7.6 for the test procedures.

Table 7.5: High-Voltage Open Operation

Objective: Verify capacitor breaker opens for high-voltage conditions.					
Specific instruction: Ensure system is not in lockout (T06 LED).					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. System with nominal voltage and current conditions: A = 69 V ∠0° VB = 69 V ∠–120° VC = 69 V ∠+120° 2. Controller in AUTO and LOCAL mode. 3. Voltage control enabled. 4. Breaker is closed.	1. Shed the following loads to generate a high-voltage condition: LD32, LD33, LD35, LD37, LD49, LD50	1.a. Countdown timer starts for 1 s. 1.b. **OPEN COMMAND** LED blinks red. 1.c. **OPENED** LED ON after successful open operation.	Refer to Figure 7.12 and Figure 7.13.	Y	
Test notes: No operation in AUTO and SUPY mode. Observe system voltage profile after the switching operation. Refer to Appendix A for C310 circuit one-line diagram.					

Results/observations: Loads LD32, LD33, LD35, LD37, LD49, and LD50 were shed to simulate a high-voltage condition to observe the capacitor bank switching operation. It is observed that the capacitor bank controller verified if the high-voltage condition existed for a minimum of 1 second (user-settable pickup time) before switching the capacitors out. The pickup time is recommended to avoid switching operations because of momentary voltage fluctuations. Once the capacitors were switched out, the voltage was observed to be within the permitted band of ±5 percent. Refer to Figure 7.12 for the voltage profile capture. The visualization software was programmed to alarm for a high-voltage condition as shown in the right side of Figure 7.12. Figure 7.13 shows the digital status. AUTO and VOLTAGE modes were enabled for this operation. No lockout conditions were present. Capacitor bank switching is captured by the transition of the CBC 52B status from 0 to 1. Accurate observations were made on the relay front-panel LED.

Figure 7.12: CBC High-Voltage Condition

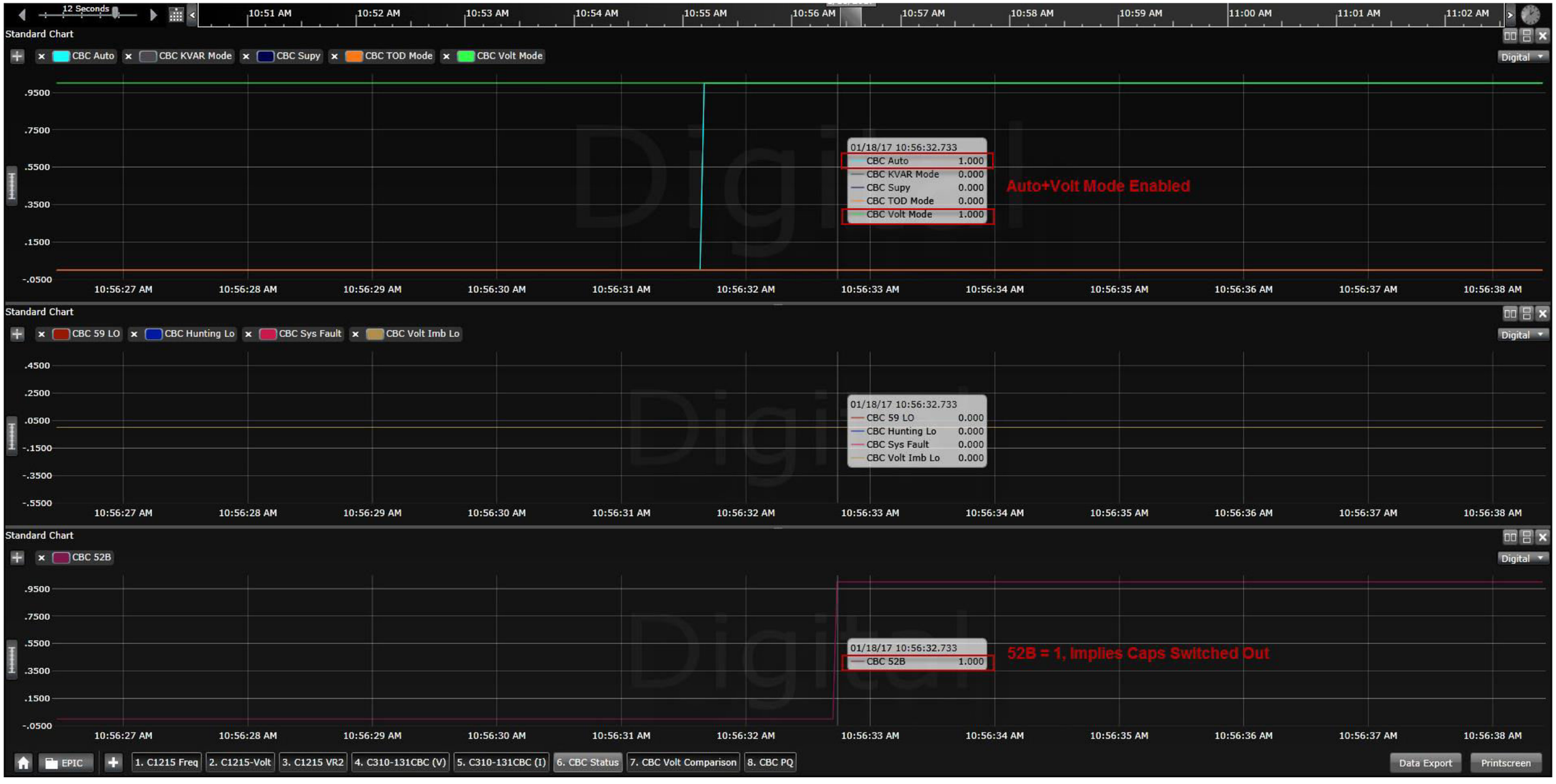


Figure 7.13: CBC High-Voltage Switching Operation

Table 7.6: Low-Voltage Close Operation

Objective: Verify capacitor breaker closes for low-voltage conditions.					
Specific instruction: Ensure system is not in lockout (T06 LED).					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. System with nominal voltage and current conditions: VA = 69 V ∠0° VB = 69 V ∠–120° VC = 69 V ∠+120° 2. Controller in AUTO and LOCAL mode. 3. Voltage control enabled. 4. Breaker is open.	1. Run load profile at 1.75 pu to simulate low-voltage conditions.	1.a. Countdown timer starts for 1 s. 1.b. **CLOSE COMMAND** LED blinks red. 1.c. **CLOSED** LED ON after successful close operation.	Refer to Figure 7.14 and Figure 7.15.	Y	
Test notes: No operation in AUTO/SUPY mode. Observe system voltage profile after the switching operation.					

Results/observations: The load profile was run at 1.75 pu to simulate a low-voltage condition to observe the capacitor bank switching operation. It is observed that the capacitor bank controller verified if the low-voltage condition existed for a minimum of 1 second (user-settable pickup time) before switching the capacitors in. The pickup time is recommended to avoid switching operations because of momentary voltage fluctuations. Once the capacitors were switched in, the voltage was observed to be within the permitted band of ±5 percent of nominal (12 kV line-to-line). Refer to Figure 7.14 for the voltage profile screen capture. The visualization software was programmed to alarm for a low-voltage condition as shown in the right side of Figure 7.14.

Figure 7.15 shows the digital status. AUTO and VOLTAGE modes were enabled for this operation. No lockout conditions were present. Capacitor bank switching is captured by the transition of the CBC 52B status from 1 to 0. Accurate observations were made on the relay front-panel LED.

Figure 7.14: CBC Low-Voltage Condition

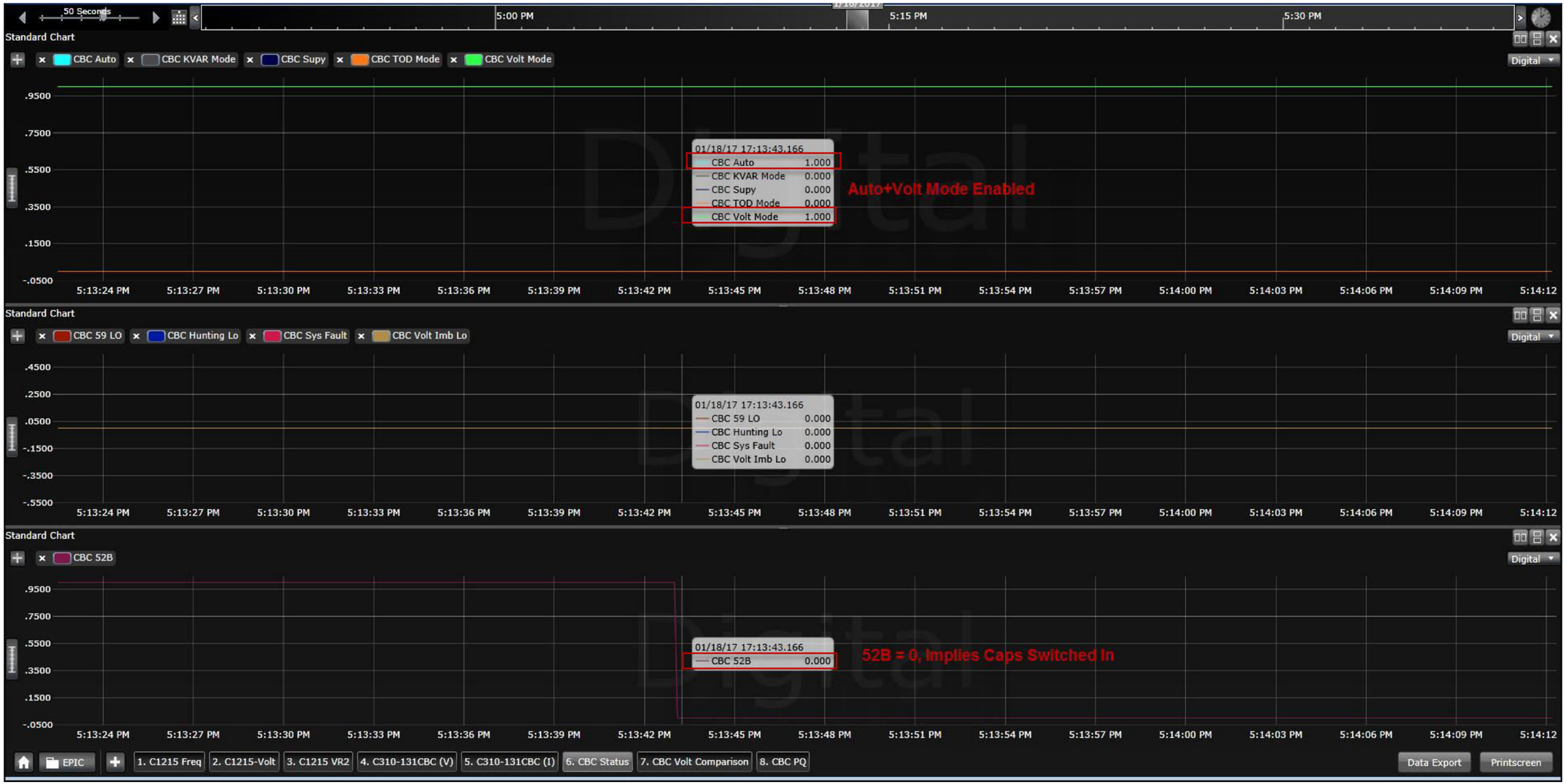


Figure 7.15: CBC Low-Voltage Switching Operation

7.2.4 Automatic KVAR Control Operation

When the controller is set to AUTO mode while KVAR Control mode is enabled via PB06, the controller automatically opens and closes the capacitor bank to maintain the KVAR load between the lagging KVAR threshold and the leading KVAR threshold. Measured reactive power for all three phases must be outside of the thresholds for the controller to operate. Refer to Table 7.7 and Table 7.8 for the test procedures.

Table 7.7: Leading KVAR Open Operation (+P)

Objective: Verify capacitor breaker opens for leading KVAR conditions.					
Specific instruction: Ensure system is not in lockout (T06 LED).					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. System with load profile at 1 pu. 2. Controller in AUTO and LOCAL mode. 3. KVAR Control enabled. 4. Breaker is closed.	1. Run load profile at 0.1 pu to simulate lead KVAR conditions.	1.a. Countdown timer starts for 1 s. 1.b. **OPEN COMMAND** LED blinks red. 1.c. **OPENED** LED ON after successful open operation.	Refer to Figure 7.16, Figure 7.17, and Figure 7.18.	Y	
Test notes: No operation in AUTO/SUPY mode. Observe system voltage profile after switching operation.					

Results/observations: The load profile was run at 0.1 pu to simulate a lead KVAR condition to observe the capacitor bank switching operation. It is observed that the capacitor bank controller verified if the lead KVAR condition existed for a minimum of 1 second (user-settable pickup time) before switching the capacitors out. The pickup time is recommended to avoid switching operations because of momentary voltage/reactive power fluctuations. Once the capacitors were switched out, the voltage was observed to be within the permitted band of ±5 percent nominal (12 kV line-to-line). Refer to Figure 7.16 and Figure 7.17 for the PQ and voltage profile, respectively. The visualization software was programmed to alarm for a lead KVAR condition as shown in the right side of Figure 7.16.

Figure 7.18 shows the digital status. AUTO and KVAR modes were enabled for this operation. No lockout conditions were present. Capacitor bank switching is captured by the transition of the CBC 52B status from 0 to 1. Accurate observations were made on the relay front-panel LED.

Figure 7.16: CBC Lead KVAR Condition – PQ Plot

Figure 7.17: CBC Lead KVAR Condition – Voltage Plot

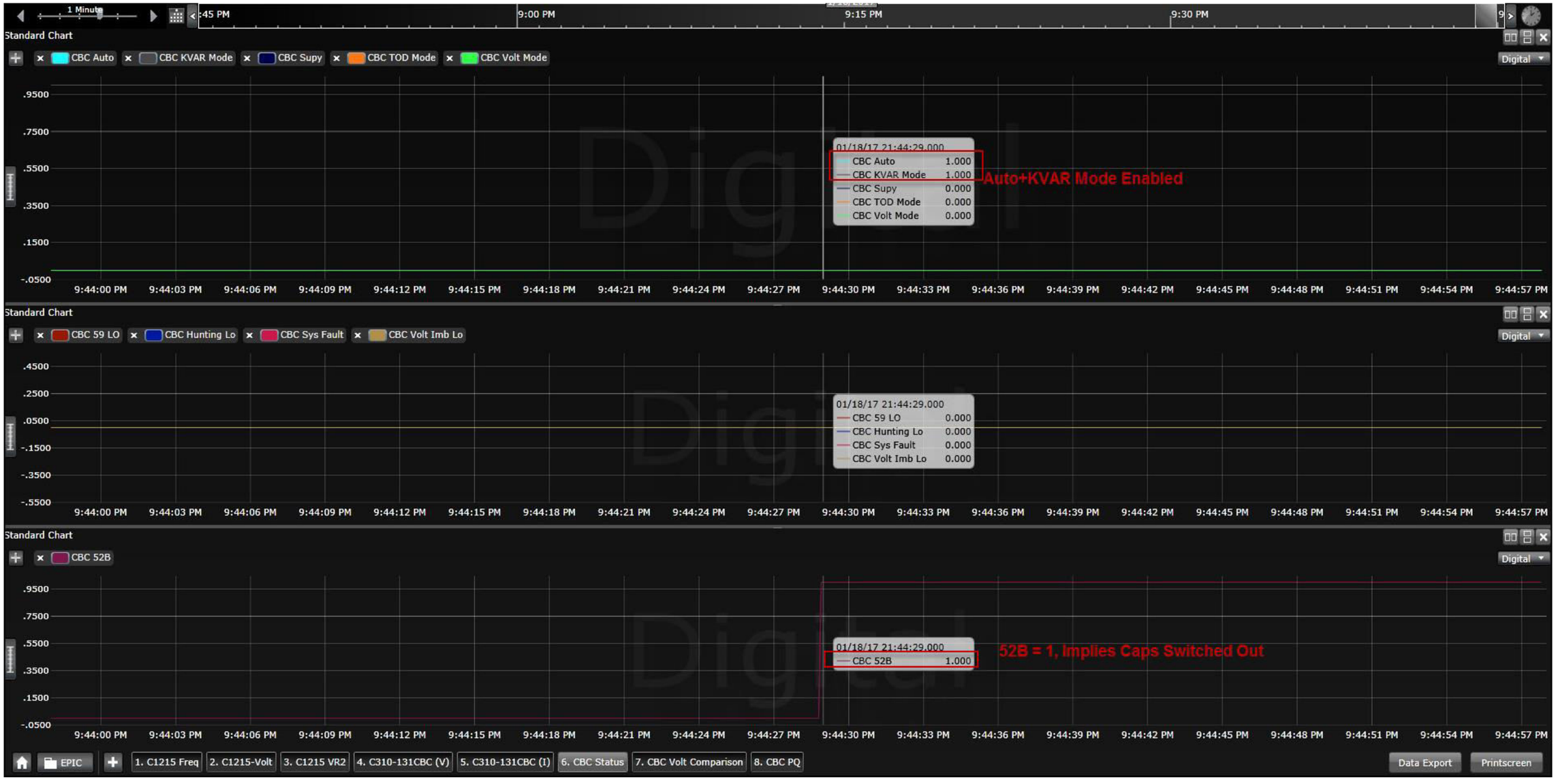


Figure 7.18: CBC Lead KVAR Switching Operation

Table 7.8: Lagging KVAR Close Operation (+P)

Objective: Verify capacitor breaker closes for lagging KVAR conditions.					
Specific instruction: Ensure system is not in lockout (T06 LED).					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. System with load profile at 1 pu. 2. Controller in AUTO and LOCAL mode. 3. Voltage control enabled. 4. Breaker is opened.	1. Continue to run load profile at 1 pu and observe for lag KVAR conditions.	1.a. Countdown timer starts for 1 s. 1.b. **CLOSE COMMAND** LED blinks red. 1.c. **CLOSED LED** ON after successful close operation.	Refer to Figure 7.19, Figure 7.20, and Figure 7.21.	Y	
Test notes: No operation in AUTO/SUPY mode. Observe system voltage profile after the switching operation.					

Results/observations: The load profile was run at 1 pu to simulate a lag KVAR condition to observe the capacitor bank switching operation. It is observed that the capacitor bank controller verified if the lag KVAR condition existed for a minimum of 1 second (user-settable pickup time) before switching the capacitors in. The pickup time is recommended to avoid switching operations because of momentary voltage/reactive power fluctuations. Once the capacitors were switched in, the voltage was observed to be within the permitted band of ±5 percent nominal (12 kV line-to-line). Refer to Figure 7.19 and Figure 7.20 for the PQ and voltage profiles, respectively. The visualization software was programmed to alarm for a lag KVAR condition as shown in the right side of Figure 7.21.

Figure 7.21 shows the digital status. AUTO and KVAR modes were enabled for this operation. No lockout conditions were present. Capacitor bank switching is captured by the transition of the CBC 52B status from 1 to 0. Accurate observations were made on the relay front-panel LED.

Figure 7.19: CBC Lag KVAR Condition – PQ Plot

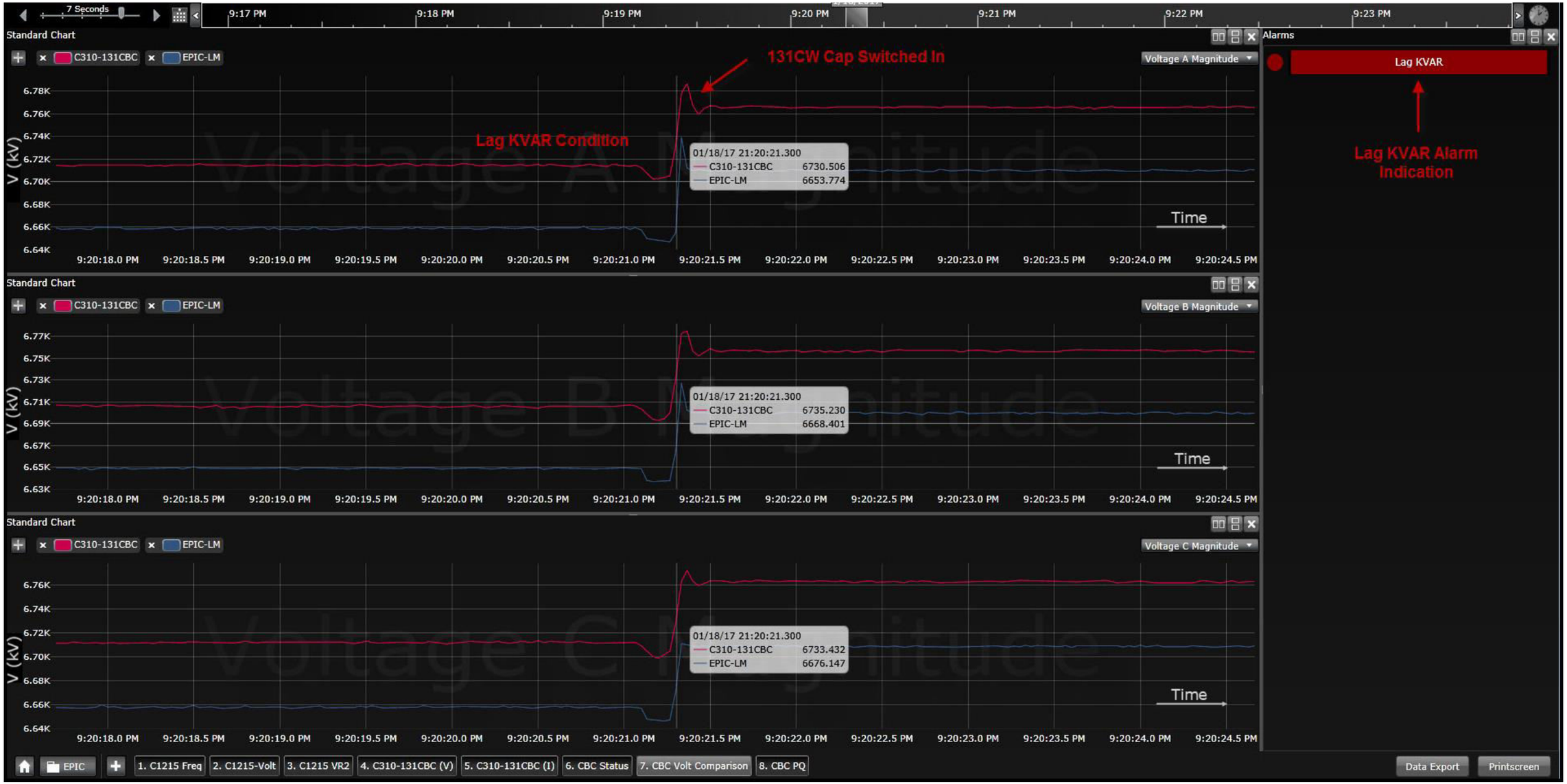


Figure 7.20: CBC Lag KVAR Condition – Voltage Plot

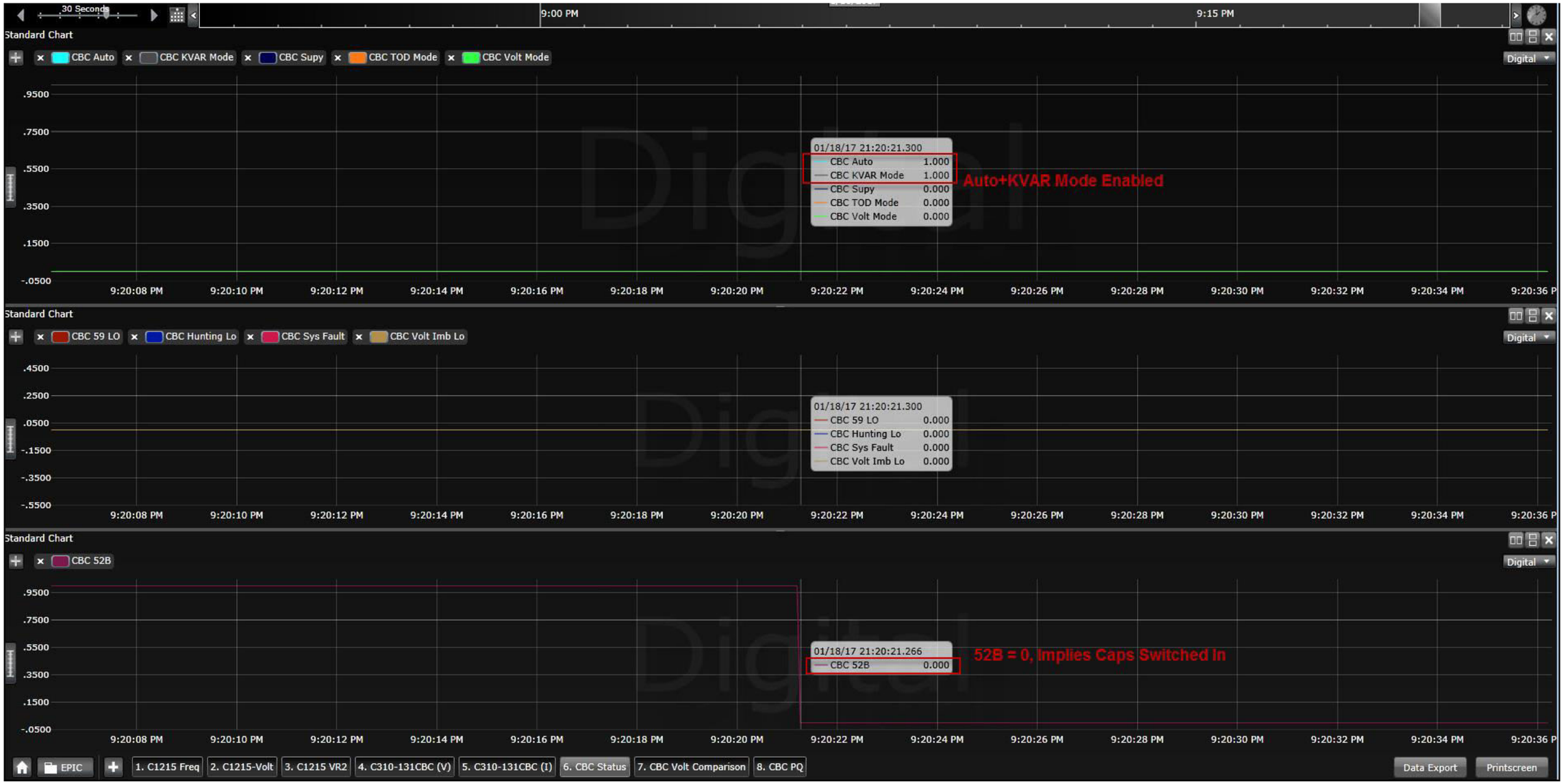


Figure 7.21: CBC Lag KVAR Switching Operation

7.2.5 Time-of-Day Operation

Based on the PQ profile provided by SDG&E for the C310 circuit, the TOD close time was selected as 14:00:00 hours and the TOD open time was selected as 05:00:00 hours to maintain a smooth load profile. Refer to Figure 7.22.

When the controller is set to AUTO mode while TOD Control is enabled via PB07, the controller opens or closes the capacitor bank based on the TOD set point. Refer to Table 7.9 and Table 7.10 for the test procedures.

Table 7.9: TOD Close Operation

Objective: Verify capacitor breaker closes at TOD start time.					
Specific instruction: Ensure system is not in lockout (T06 LED).					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. System with nominal load profile. 2. Controller in AUTO and LOCAL mode. 3. TOD Control enabled. 4. Breaker is open.	1. Set time to 13:59:50.	1. The breaker should close immediately as soon as the time is 14:00:00.	Refer to Figure 7.22 and Figure 7.23.	Y	
Test notes: Observe relay SER.					

Results/observations: The model is run at nominal load for the TOD close test. The IRIG-B connection was removed for this test to change the internal clock of the controller. The time was set at 13:59:50 hours. The capacitor bank breaker closed as soon as the time turned to 14:00:00 hours.

Figure 7.23 shows the digital status. TOD mode was enabled for this operation, shown by “TODMODE” as enabled in Figure 7.23 . Capacitor bank switching is captured by CAPBRK Relay Word bit status as Closed. Accurate observations were made on the relay front-panel LED.

Recommendations: It is recommended to observe the load profile and PQ distribution over 24 hours and over different days (for example, weekends, weekdays, and different seasons) before setting up the TOD close time. Dedicated TOD programs can run in the controller for weekdays and weekends.

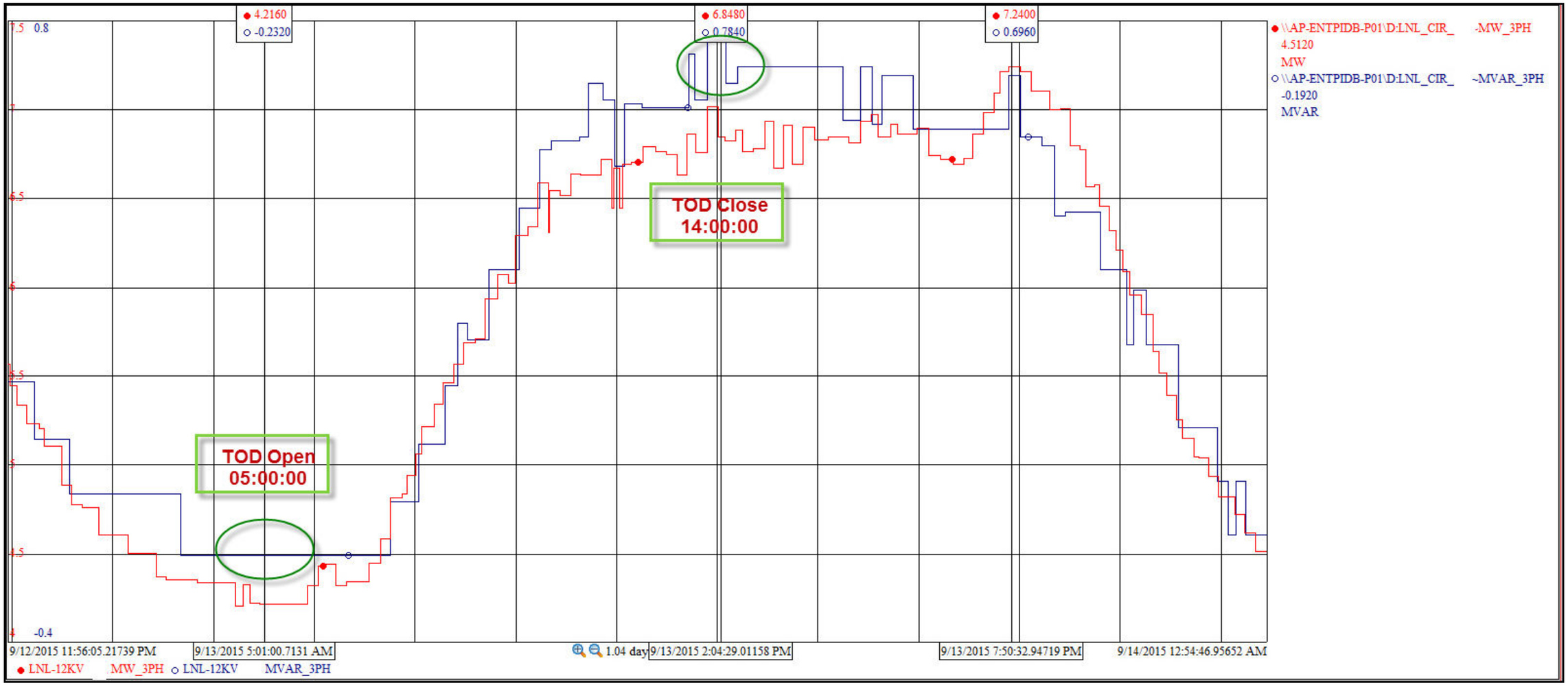


Figure 7.22: Circuit PQ Profile Over 24 Hours

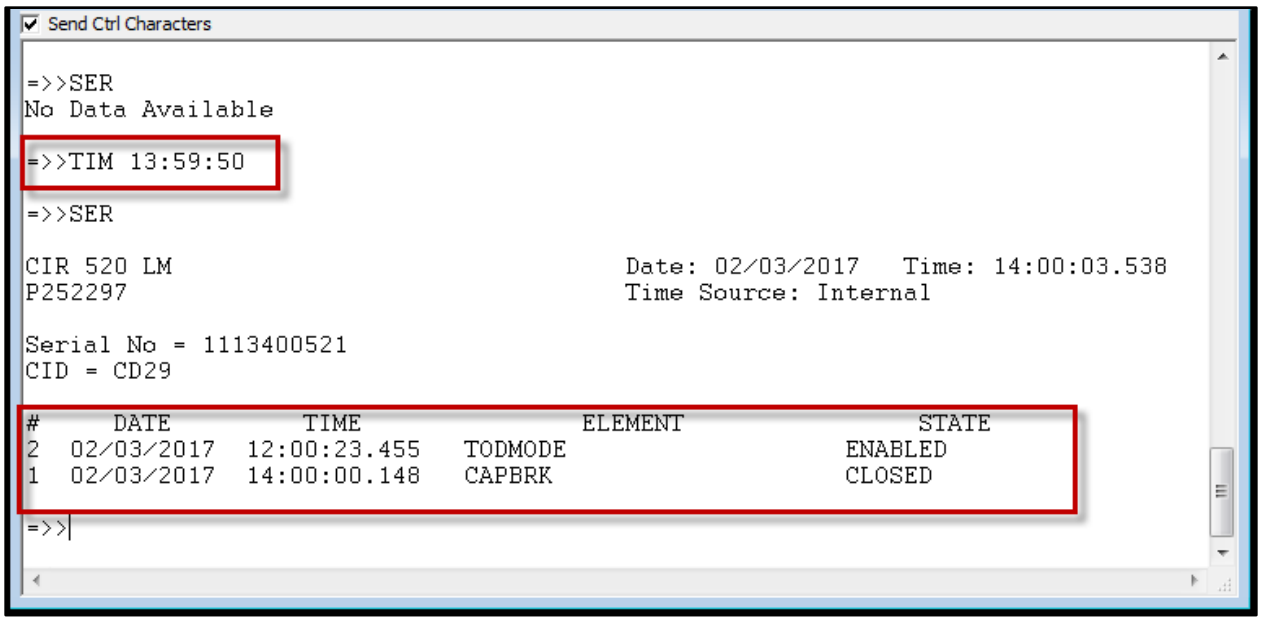


Figure 7.23: CBC TOD Close Switching Operation at 14:00:00 Hours

Table 7.10: TOD Open Operation

Objective: Verify capacitor breaker opens at TOD end time.					
Specific instruction: Ensure system is not in lockout (T06 LED).					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. System with nominal load profile. 2. Controller in AUTO and LOCAL mode. 3. TOD Control enabled. 4. Breaker is closed.	1. Set Time to 04:59:50.	1.a. The breaker should open immediately as soon as the time is 05:00:00.	Refer to Figure 7.22 and Figure 7.24.	Y	
Test notes: Observe system voltage profile after switching operation.					

Results/observations: The model is run at nominal load for the TOD open test. The IRIG-B connection was removed for this test to change the internal clock of the controller. The time was set at 04:59:50 hours. The capacitor bank breaker opened as soon as the time turned to 05:00:00 hours.

Figure 7.24 shows the digital status. The TOD mode was enabled for this operation shown by "TODMODE" as enabled in Figure 7.24 . Capacitor bank switching is captured by CAPBRK Relay Word bit status as Opened. Accurate observations were made on the relay front-panel LED.

Recommendations: It is recommended to observe the load profile and PQ distribution over 24 hours and over different days (for example, weekends, weekdays, and different seasons) before setting up the TOD open time. Dedicated TOD programs can run in the controller for weekdays and weekends.

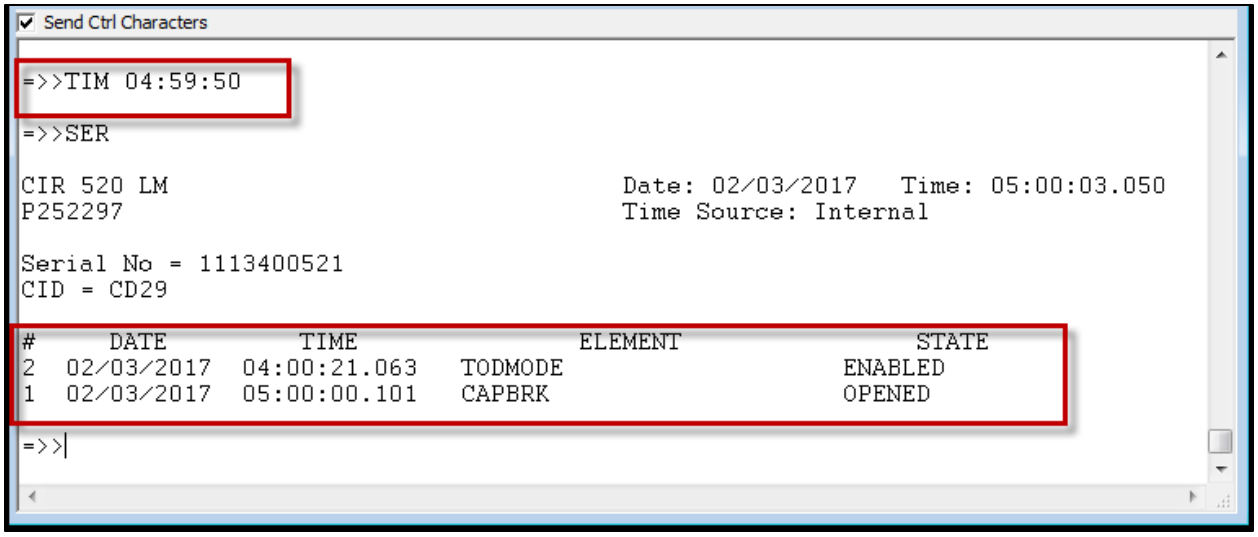


Figure 7.24: CBC TOD Open Switching Operation at 05:00:00 Hours

7.2.6 Overvoltage Lockout

Overvoltage lockout is essential for the protection of the capacitor bank. In case of an overvoltage condition, the capacitor breaker should trip and issue a lockout, thereby, preventing all automatic switching operations until the lockout is cleared by the operator. Refer to Table 7.11 for the test procedure.

Table 7.11: Overvoltage Lockout

Objective: Simulate overvoltage condition and verify capacitor breaker opens.					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. System with nominal voltage and current conditions: VA = 69 V ∠0° VB = 69 V ∠–120° VC = 69 V ∠+120° 2. Breaker closed.	1. Raise test set voltage by 12%. VA = 77 V ∠0° VB = 77 V ∠–120° VC = 77 V ∠+120°	1.a. Breaker opens. 1.b. Controller goes to lockout – LED06 ON.	Refer to Figure 7.25 and Figure 7.26.	Y	
Test notes: Overvoltage trip should be allowed in all possible combinations of operating modes because it is a protection lockout. Once a lockout is declared, all automatic operations should be inhibited.					

Results/observations: The load profile was run at 1 pu. System voltage was increased with a slider in RTDS RunTime to simulate a three-phase overvoltage condition. The controller verified if the overvoltage condition existed for a minimum of 1 second (user-settable pickup time) before switching the capacitors bank out. Refer to Figure 7.25. The visualization software was programmed to alarm for overvoltage condition as shown in the right side of Figure 7.26.

Figure 7.26 shows the digital status. The overvoltage lockout alarm is enabled. Capacitor bank switching is captured by the transition of the CBC 52B status from 0 to 1. Accurate observations were made on the relay front-panel LED.

Figure 7.25: CBC Overvoltage Condition

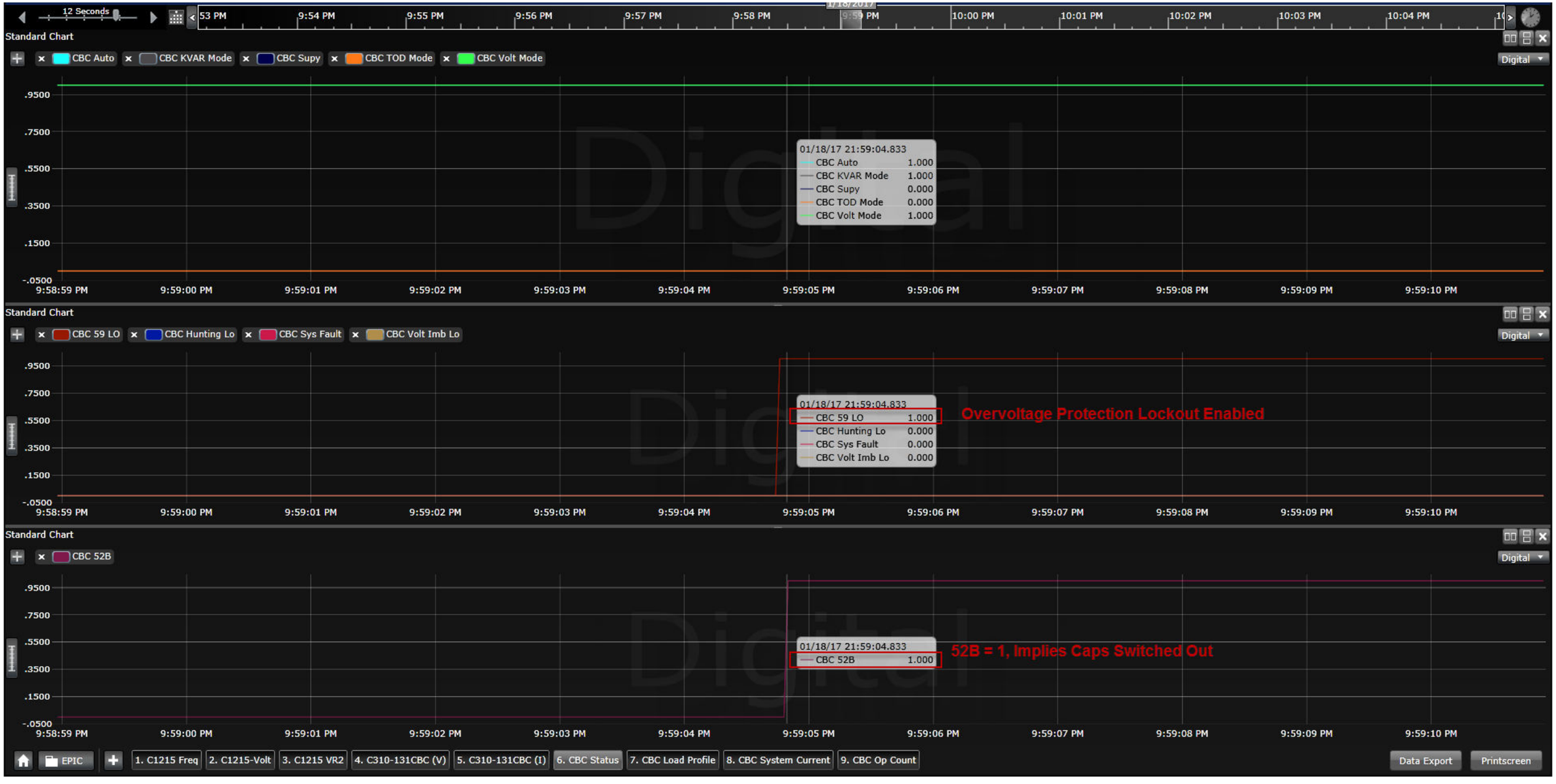


Figure 7.26: CBC Overvoltage Condition Lockout Operation

7.2.7 Voltage Imbalance Lockout

Voltage imbalance lockout is essential for the protection of the capacitor bank. In case of an imbalance condition, the capacitor breaker should trip and issue a lockout, thereby, preventing all automatic switching operations until the lockout is cleared by the operator. Refer to Table 7.12 for the test procedure.

Table 7.12: Voltage Imbalance Lockout

Objective: Simulate voltage imbalance and verify that the capacitor breaker opens.					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. System with nominal voltage and current conditions: VA = 69 V ∠0° VB = 69 V ∠–120° VC = 69 V ∠+120 2. Breaker closed.	1. Lower Phase A voltage to cause an imbalance greater than 3%.	1.a. Breaker opens. 1.b. Controller goes to lockout – LED06 ON.	Refer to Figure 7.27, Figure 7.28, and Figure 7.29.	Y	
Test notes: The voltage imbalance threshold is at 3 percent. Voltage imbalance trip should be allowed in all possible combinations of operating modes. Once lockout is declared, all automatic operations should be inhibited.					

Results/observations: The load profile was run at 1 pu. Phase A voltage was increased with a slider in RTDS RunTime to simulate a voltage imbalance condition. The controller verified if the voltage imbalance condition existed for a minimum of 1 second (user-settable pickup time) before switching the capacitors out. Refer to Figure 7.27.

Figure 7.28 captures the percentage voltage imbalance registered by the relay. The visualization software was programmed to alarm for a voltage imbalance condition as shown in the right side of Figure 7.27.

Figure 7.29 shows the digital status. Voltage imbalance lockout alarm is enabled. Capacitor bank switching is captured by the transition of the CBC 52B status from 0 to 1. Accurate observations were made on the relay front-panel LED.

Figure 7.27: CBC Voltage Imbalance Condition

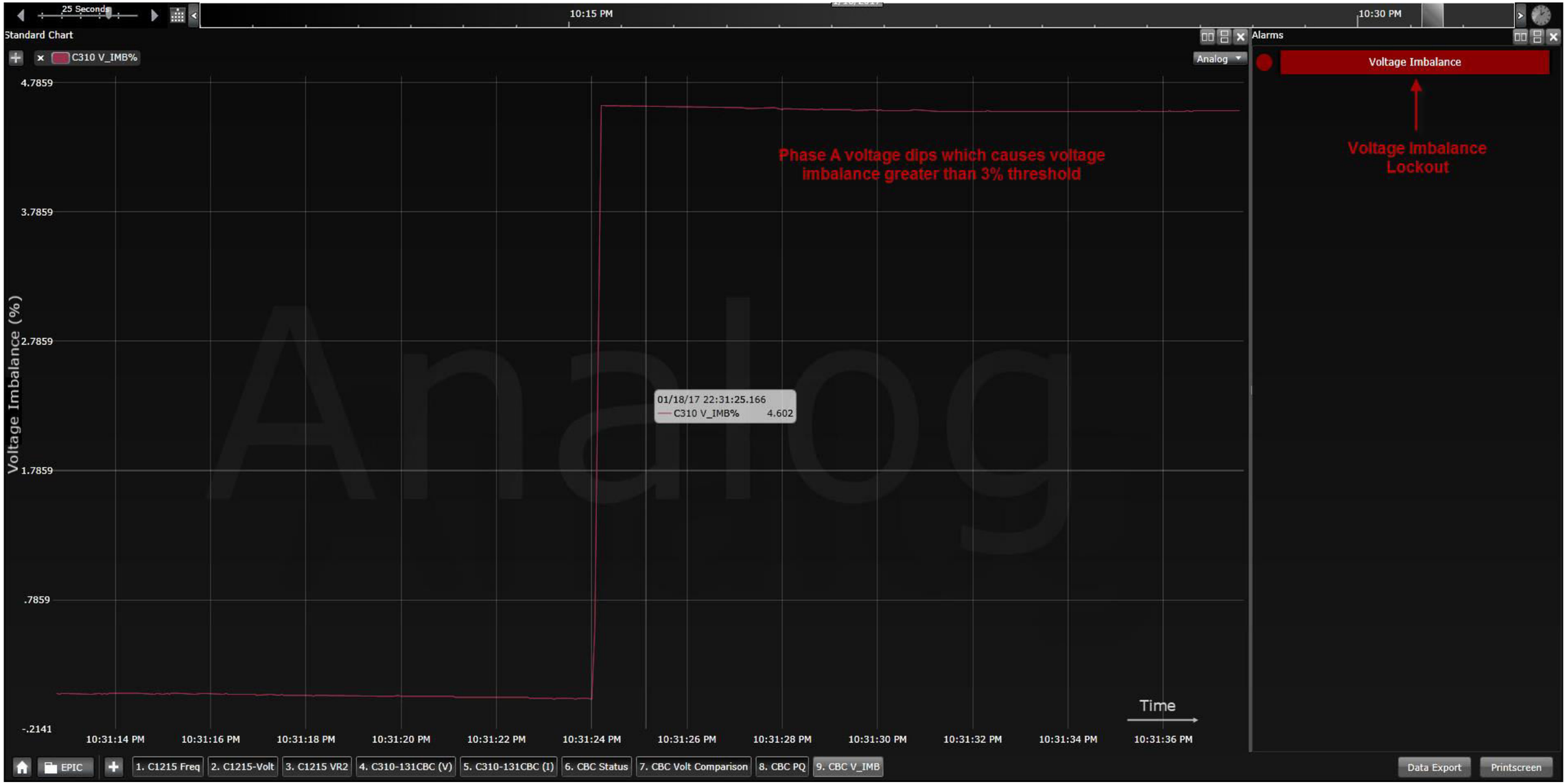


Figure 7.28: CBC Voltage Imbalance Percentage

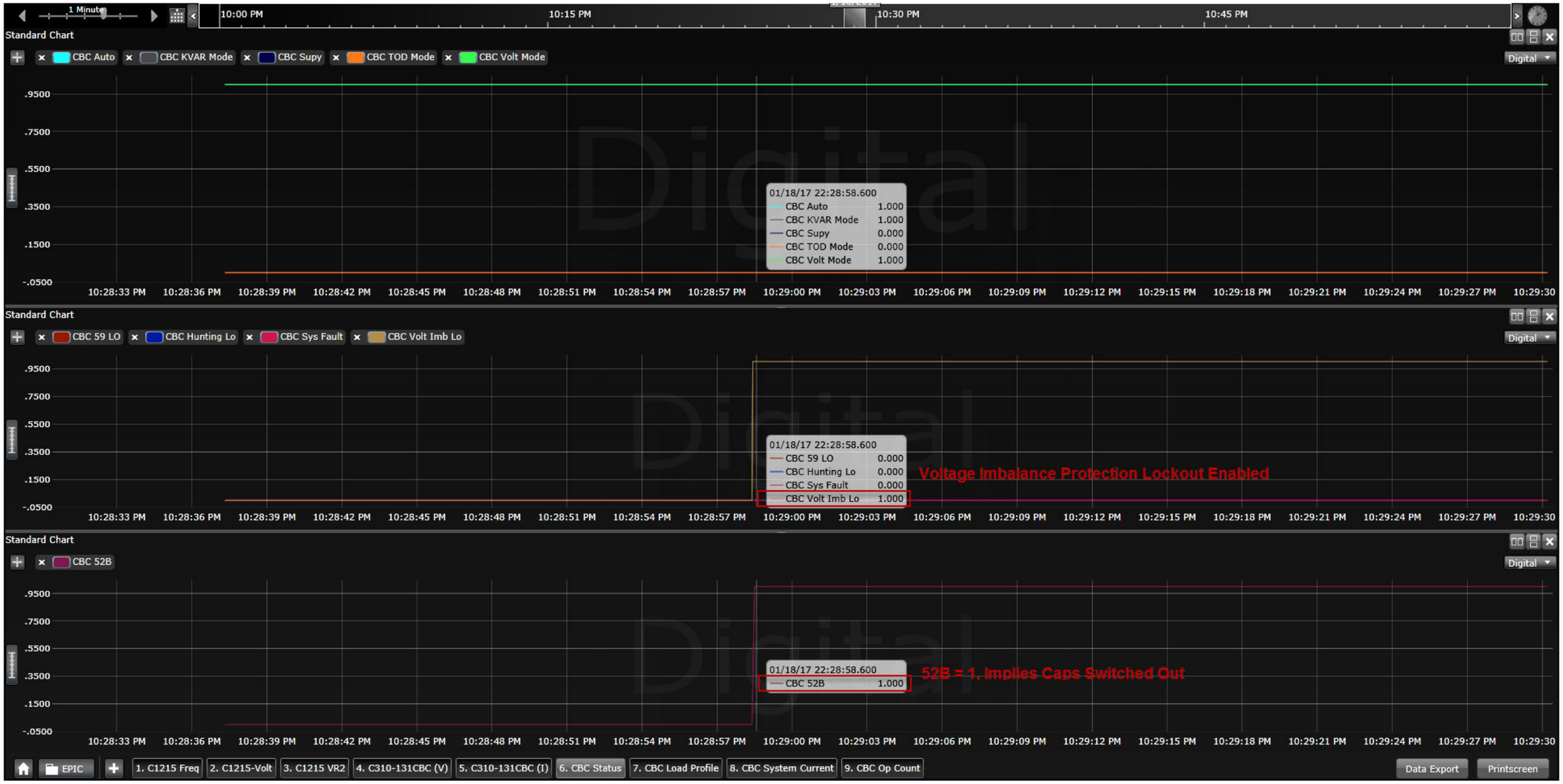


Figure 7.29: CBC Voltage Imbalance Lockout Operation

7.2.8 High-Current Condition

The capacitor bank controller is programmed for a high-current alarm indication. If the system current exceeds the set threshold, the controller alarms as long as a high-current condition is present. A high-current condition does not cause the capacitor breaker to open or inhibit any automatic switching operations. It is understood that the upstream system protection will arrest the high-current condition in the system. Refer to Table 7.13 for the test procedure.

Table 7.13: High-Current Condition

Objective: Simulate high current and verify alarm indication.					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. Run the system with nominal voltage and current. 2. Breaker closed.	1. Raise test set current to more than 600 A primary.	1. Controller indicates high-current condition on target LED05.	Refer to Figure 7.30 and Figure 7.31.	Y	
Test notes: The high-current condition does not inhibit LOCAL or AUTO operations. LOCAL reset: Reset the fault latch by pressing the **RESET** pushbutton. Automatic reset: If the fault condition clears, the fault latches and the indication LED will clear automatically after 10 minutes.					

Results/observations: The load profile was run at 1 pu. System current was increased with the help of a slider in RTDS RunTime to simulate a high-current condition. The controller alarmed for this condition as shown in Figure 7.30.

Figure 7.31 shows the digital status. A high-current alarm is enabled. It can also be observed that the alarm automatically resets after 10 minutes provided the high-current condition is not present in the system. Accurate observations were made on the relay front-panel LED.

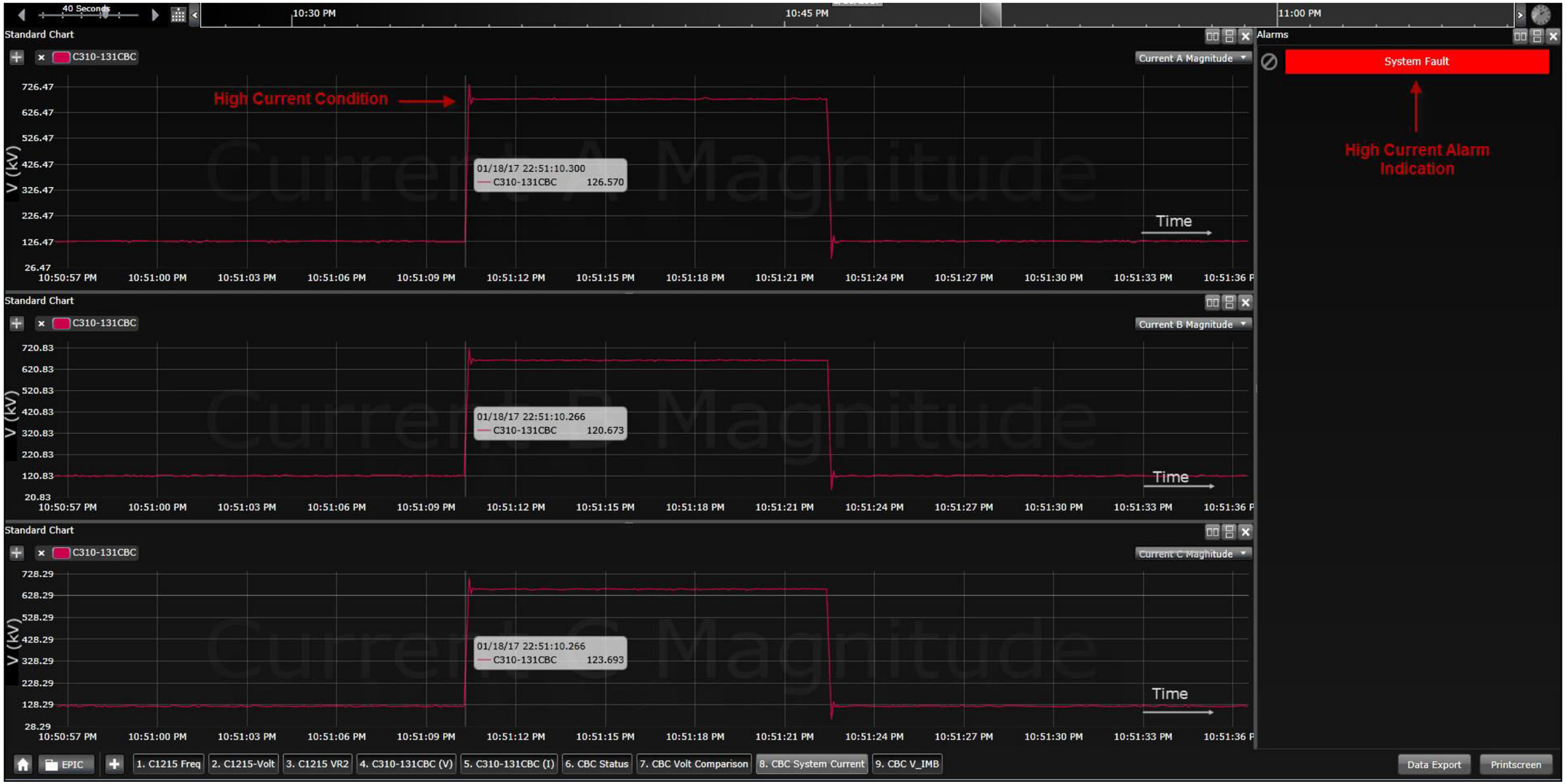


Figure 7.30: CBC High-Current Condition

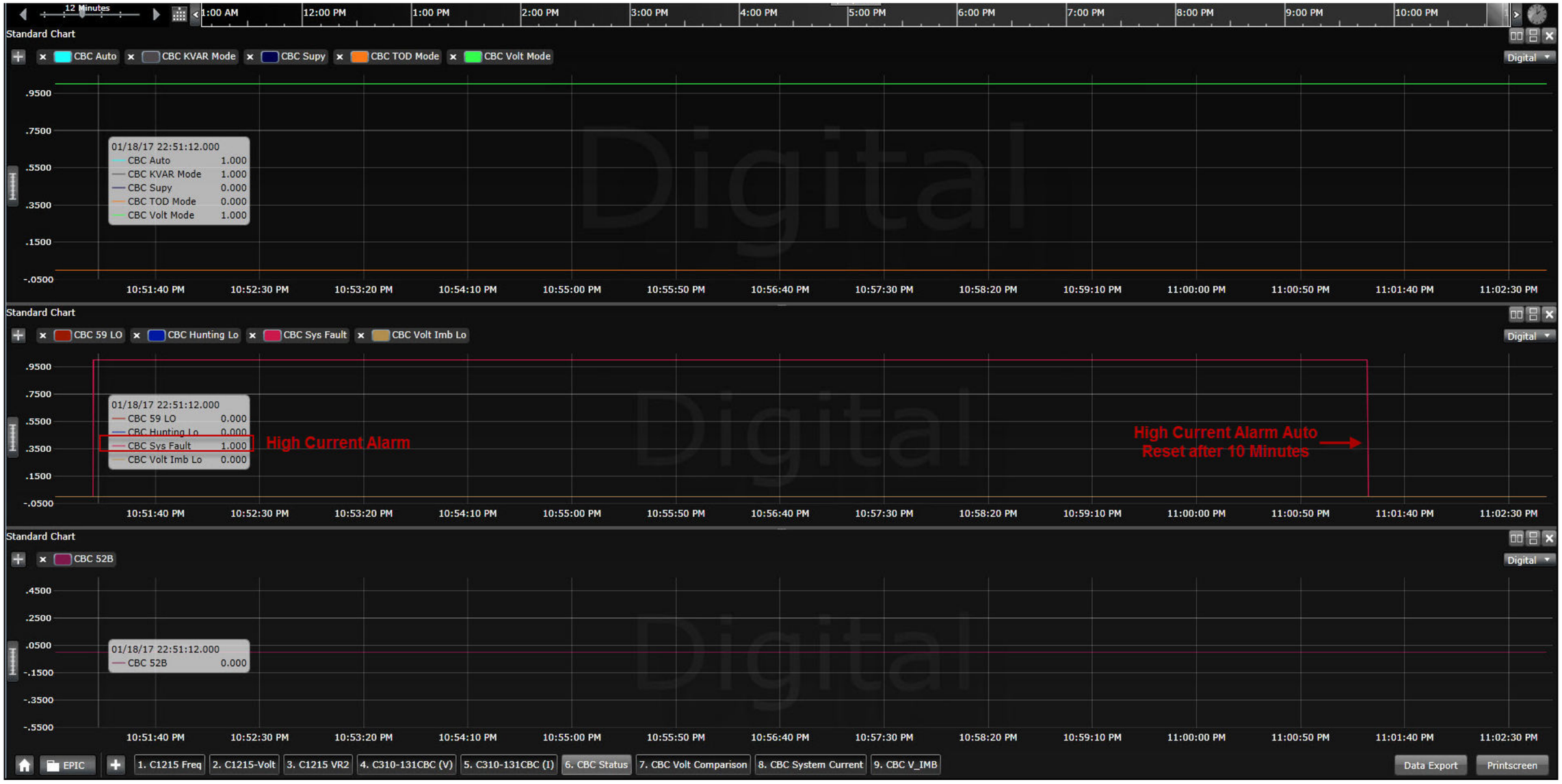


Figure 7.31: CBC High-Current Alarm Indication and Automatic Reset

7.2.9 Hunting Lockout

When the controller is set to AUTO mode, the hunting feature inhibits further operations if a specified number of open and close operations occur within a specified time window, which is known as the hunting time window. Refer to Table 7.14 for the test procedure.

Table 7.14: Hunting Lockout

Objective: Verify hunting lockout is asserted once the counts threshold is crossed.					
Specific instruction: Ensure system is not in lockout (T06 LED).					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. System with nominal conditions. 2. Controller in AUTO mode. 3. Voltage control enabled.	1. Set hunting window = 5 min. 2. Set hunting count = 3. 3. Trigger breaker open and close operations via abnormal voltage.	1.a. Hunting lockout not asserted after the 2nd operation. 1.b. Hunting lockout asserted after the 3rd operation. 1.c. No further close/open operations are allowed. 1.d. The LCD displays Hunting Lockout.	Refer to Figure 7.32.	Y	
Test notes: The hunting window and hunting count threshold are modified to decrease the hunting time window and the hunting count for testing.					

Results/observations: Three consecutive voltage switching operations were carried out in a window of 5 minutes (as set via hunting window). The first was a high-voltage open operation, followed by a low-voltage close operation, followed by a high-voltage open operation. All three operations were captured in Figure 7.32. It can be observed that a hunting lockout is issued after the third operation because the hunting count is set to three.

Hunting lockout should prevent any further automatic operations. The alarm can be reset locally via operator controlled reset pushbutton on the relay. Options should be provided to reset this automatically after a set time or remotely via SCADA.

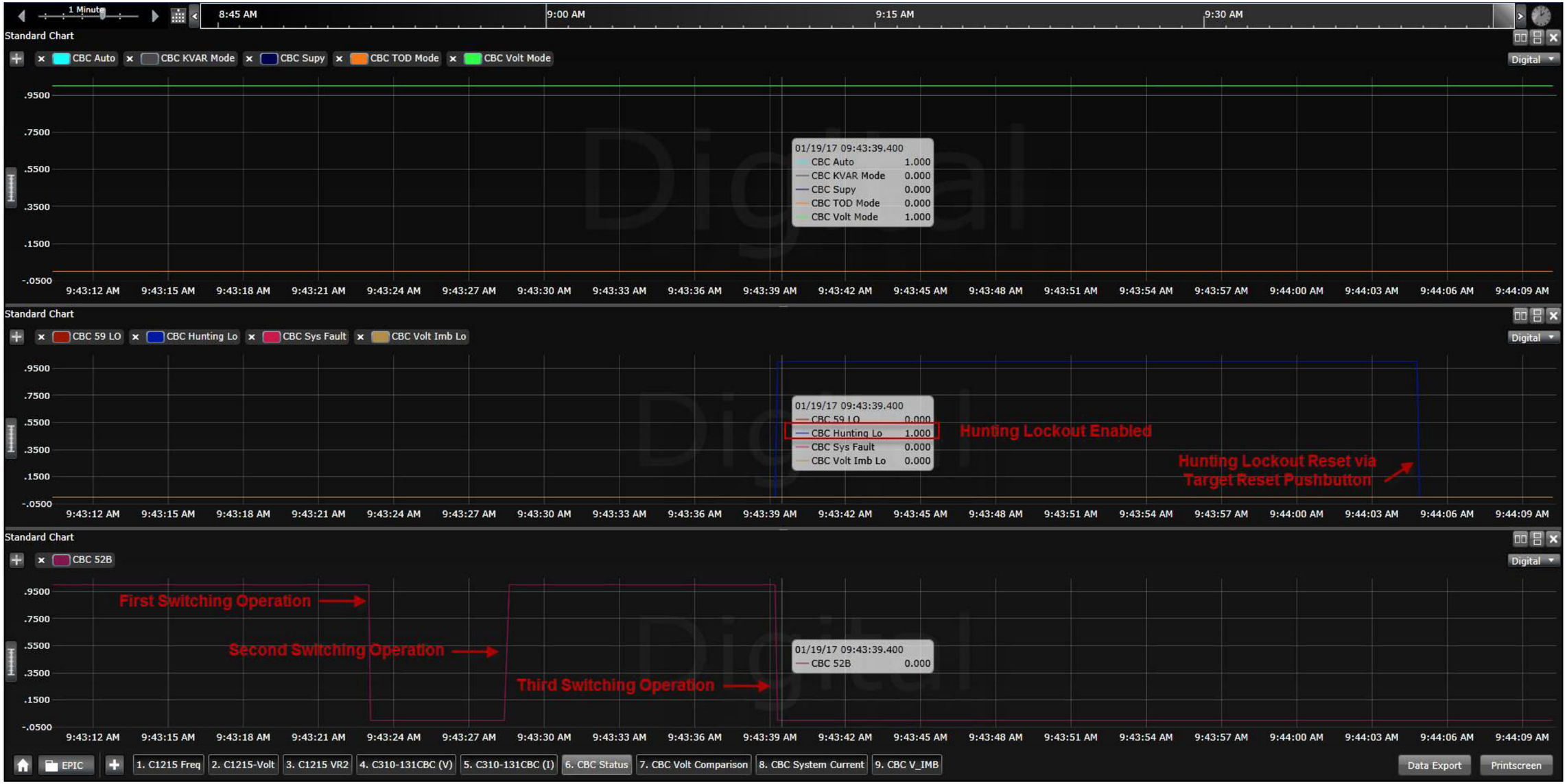


Figure 7.32: CBC Hunting Lockout

Hunting Reset: Hunting lockout can be reset as follows:

Local:

1. Ensure the controller is in LOCAL mode.
2. Press **RESET**.
3. The hunting lockout display point should clear out.

7.2.10 Operations Counters

There are three operations counters:

1. Counts since installation.
2. Yearly counts.
3. Daily counts.

Operations Counter Reset

Local Reset: Press the PB04 and **RESET** pushbuttons together for 5 seconds.

Automatic Reset: Yearly counter resets when DAYY (day of year) = 1. Daily counter resets when minutes since midnight (MINSM) = 0.

Results/observations: The controller is programmed to keep a count of the number of switching operations since installation, and on a daily and a yearly basis. This information can be vital for equipment monitoring and maintenance. Figure 7.33 shows the count registered. This can be reset locally via the **Target Reset** pushbutton on the relay.

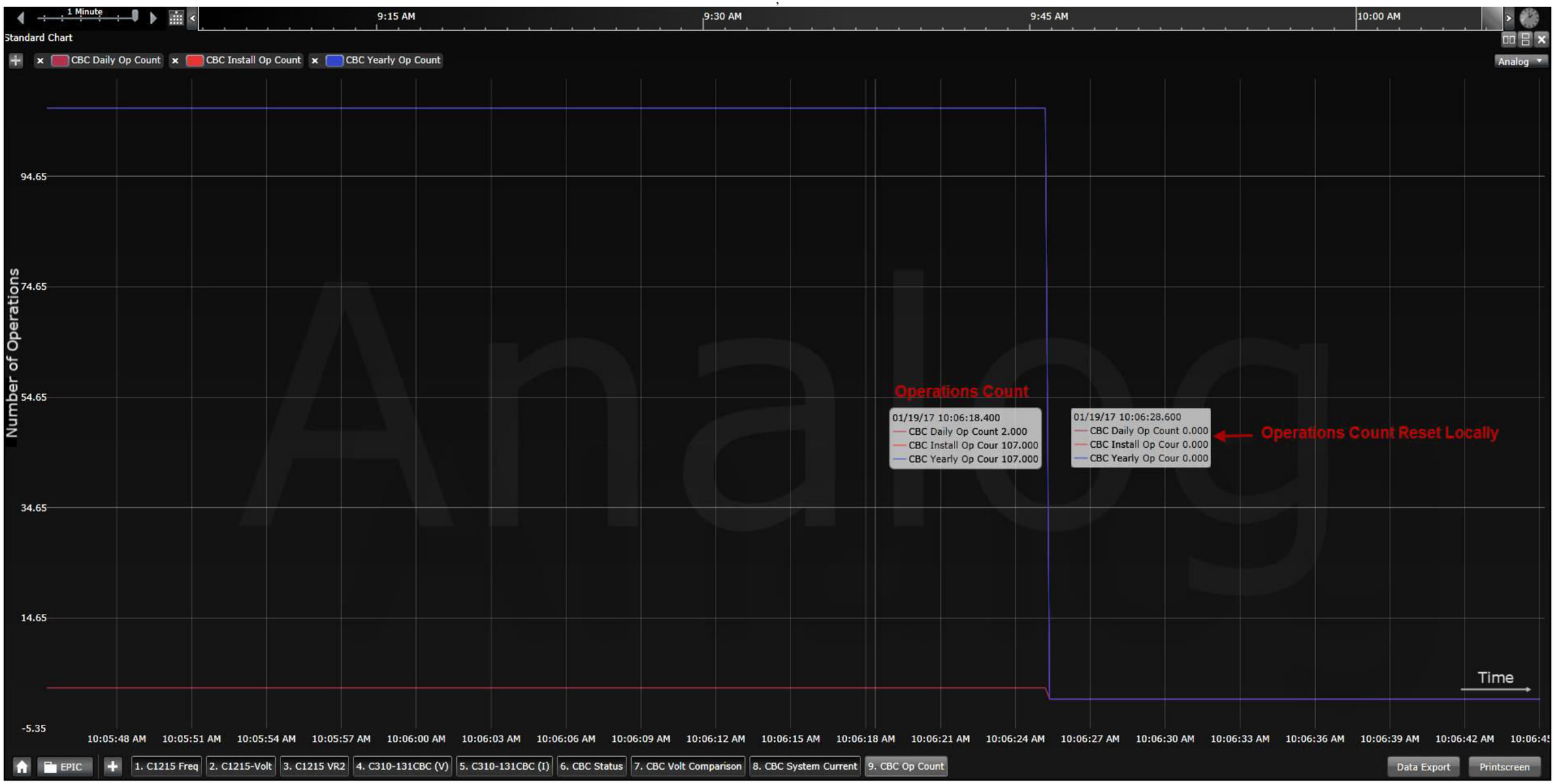


Figure 7.33: CBC Operations Counter

8 HIGH-IMPEDANCE FAULT DETECTION

High-impedance faults (HIF) are short-circuit faults with fault currents typically smaller than what traditional overcurrent relays can detect. The main causes of HIFs are tree branches touching a phase conductor, dirty insulators causing a flashover between the phase conductors and the ground, or downed conductors. Significantly small fault current values make the detection of high-impedance faults challenging. Special algorithms may be required to detect and isolate the circuit during high-impedance faults.

The Advanced Recloser Control used in this study provides the intelligence to a recloser that allows reconfiguration of a distribution system and maintenance of reliable service to as many power networks as possible in the event of a fault. In addition, the recloser control provides high-impedance fault detection and protection capabilities. The tests performed in this section demonstrate the features and functionalities available to detect high-impedance faults on distribution circuits.

Section 8.1 describes the laboratory test setup and the recloser control hardware configuration.

Section 8.2 provides an overview of HIF functionality in the recloser control.

Section 8.3 includes the procedure for testing HIFs in distribution circuits.

Section 8.4 provides a description of the HIF settings in the recloser control for laboratory testing.

Section 8.5 includes the different scenarios for testing HIFs in distribution circuits. The scenarios include faults at varying fault impedances and fault locations, and response of the high-impedance detection logic during the load profile run.

RTDS tests were carried out to study HIF detection capabilities of the recloser control at various locations of the SDG&E circuit and for faults with different fault impedances. The testing includes two scenarios. The first scenario was Auto and Remote Toggle – From Local Control (Section 8.5.1). The second scenario was HIF detection (Section 8.5.2). Refer to Figure 8.1 for a simplified one-line diagram with two fault locations. A single-line-to-ground fault with an impedance of 85 ohms and duration of 200 milliseconds is simulated for these tests.

The test results are captured using a visualization software and the sequence of events.

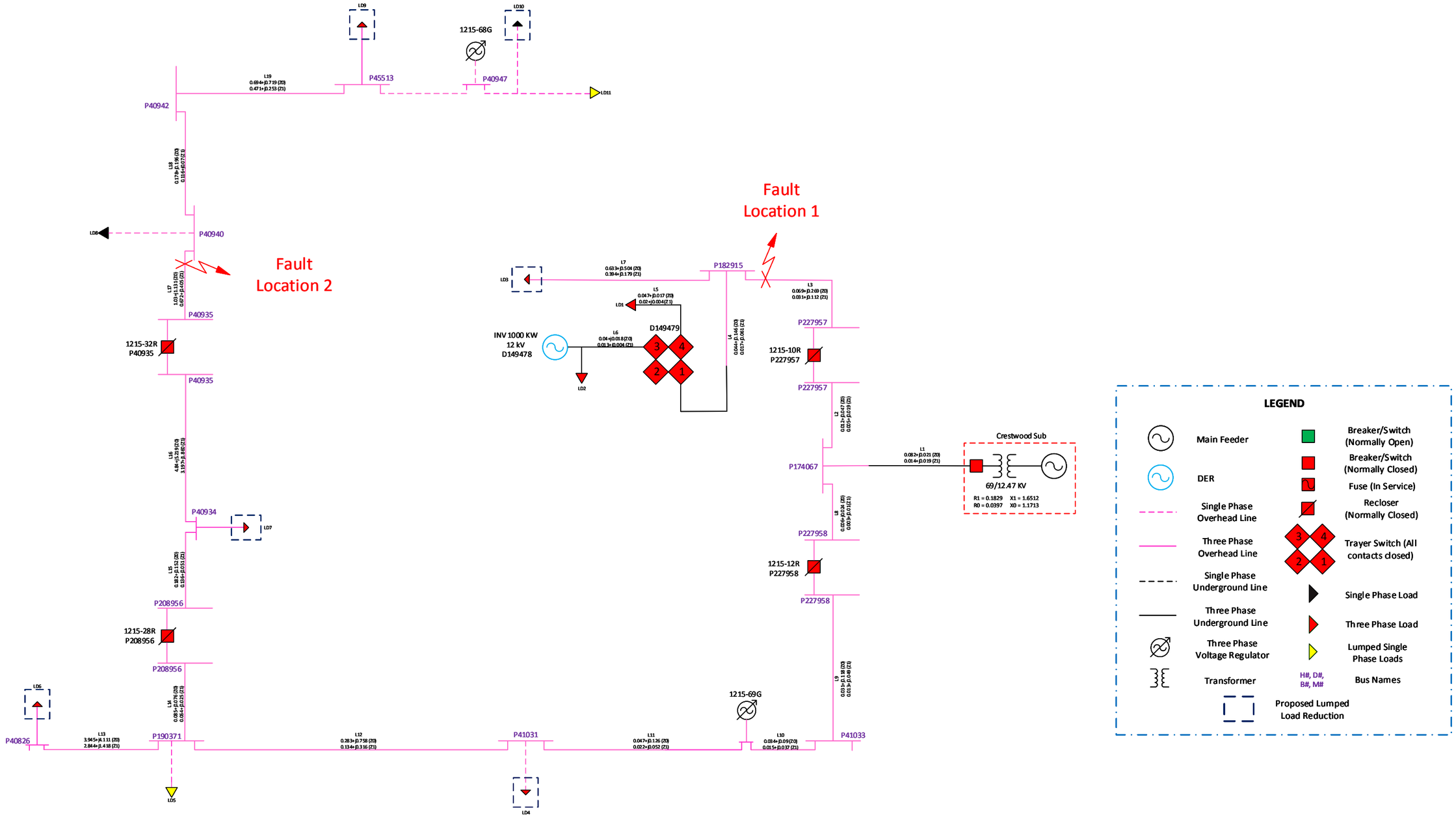


Figure 8.1: Simplified One-Line Diagram With Fault Locations

8.1 TEST SETUP

The hardware setup of the test circuit is shown in Figure 8.2. The circuit involving the recloser control is simulated on the RTDS and the recloser currents and voltages are derived from the circuit. These voltages in the low-level signal form are fed to the recloser control. The recloser control HIF logic will detect this condition and send control signals back to the RTDS to control the recloser.

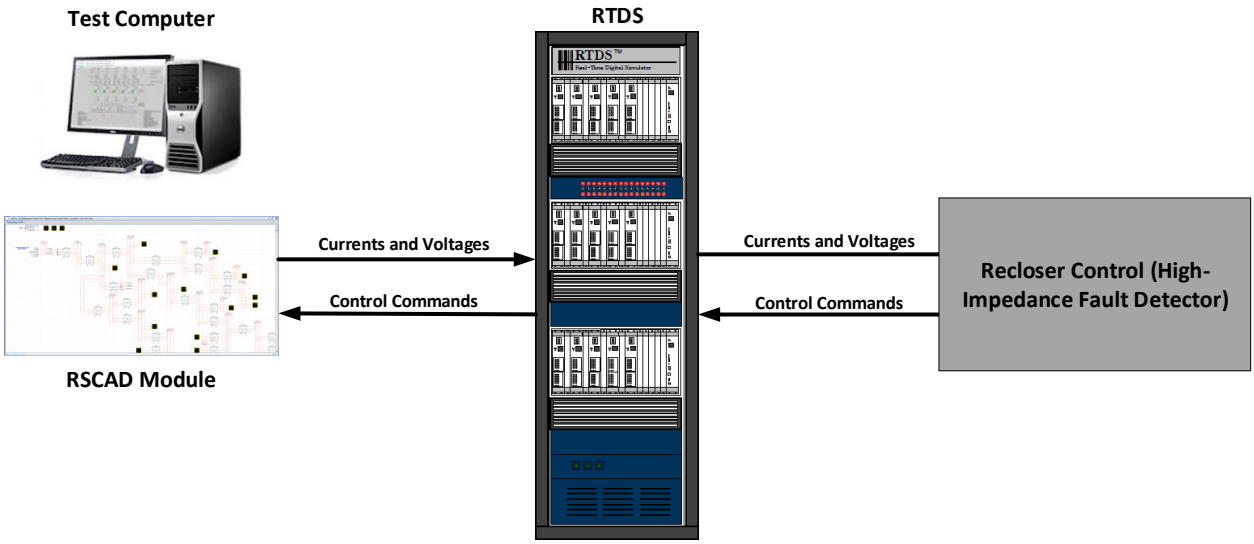


Figure 8.2: HIF Detection Test Setup

8.1.1 RTDS Interface and I/O List

Figure 8.3 illustrates the analog inputs and outputs assigned to the various channels of the RTDS GTAO card. Each of the GTAO cards represent the outputs for one recloser. For GTAO A01 (1215-10R) on the left side in Figure 8.3, Channels 1 through 3 are reserved for the A, B, and C phase currents (10RIA, 10RIB, and 10RIC, respectively). Channels 4 through 9 represent the A, B, and C voltages for the Y and Z side of the recloser (10RYA, 10RYB, 10RYC, 10RZA, 10RZB, and 10RZC, respectively). GTAO A02 (1215-32R) follows the same format.

For testing purposes, set the Relay Word bit EHIF = T (Test mode). This setting allows the HIF detection algorithm to bypass the 24-hour tuning process. For normal operation, EHIF = Y.

The recloser control indicates HIF detection through the Relay Word bits outputs detailed in Table 8.1.

Table 8.2 describes the digital outputs assignment from the recloser control to the RTDS.

Figure 8.4 shows the mapping for digital inputs and outputs, respectively, via the GTFPI card.

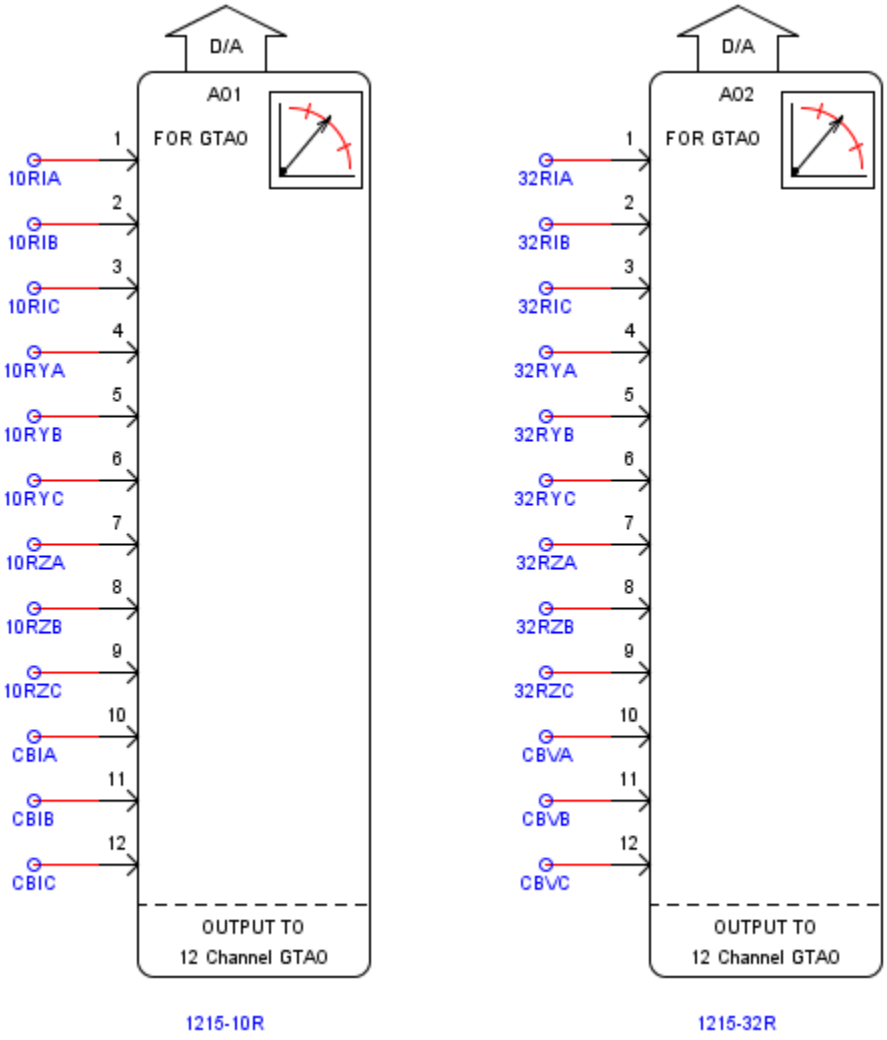


Figure 8.3: Recloser RTDS Analog Output Signals

Table 8.1: HIF Relay Word Bits

HIF Activity	Relay Word Bits
HIF SDI (nonharmonic) ALARM	HIA2_A, HIA2_B, HIA2_C
HIF SDI (nonharmonic) FAULT	HIF2_A, HIF2_B, HIF2_C
Voltage Disturbance	DVA_DIS, DVB_DIS, DVC_DIS
Disable HIF Decision Logic	DL2CLRA, DL2CLRB, DL2CLRC
Initial Tuning in Progress	ITUNE_A, ITUNE_B, ITUNE_C
Initiate Tuning Process	INI_HIF, HIFITUNE
Normal Tuning in Progress	NTUNE_A, NTUNE_B, NTUNE_C
Increase the HIF Tuning Threshold	DUPA, DUPB, DUPC
Decrease the HIF Tuning Threshold	DDNA, DDNB, DDNC
Load Reduction Detected	LRA, LRB, LRC, LR3
HIF Externally Triggered Event	HIFER
HIF Detection Mode Sensitivity	HIFMODE
HIF Event Report is being collected	HIFREC

Table 8.2: Recloser Control I/O List

Output Contact	Function
OUT101	Trip
OUT102	Close
OUT101	Trip
OUT102	Close

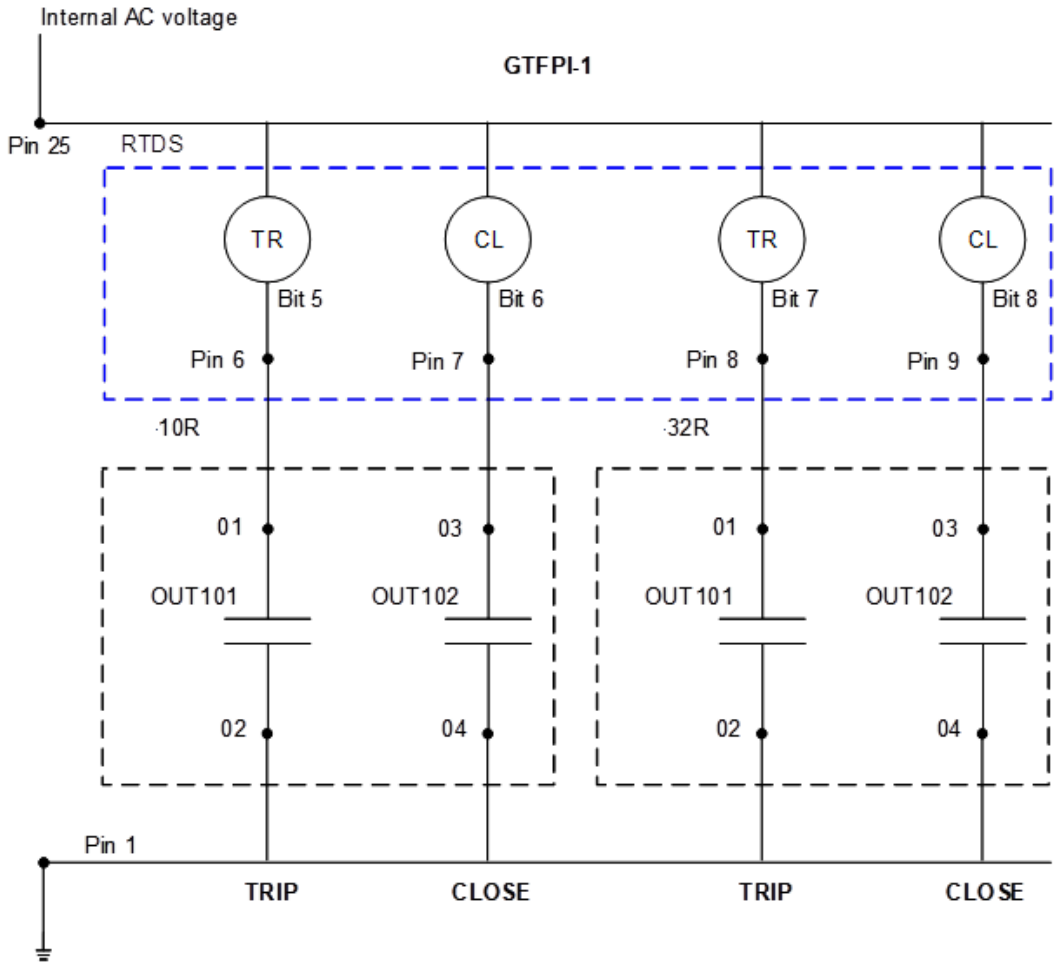


Figure 8.4: Recloser Trip and Close Digital Input Wiring

8.2 HIF OVERVIEW

HIFs are those with high resistance in the fault path. Typical causes of HIFs include trees coming into contact with overhead lines, conductors falling onto poorly conductive surfaces (asphalt, dry grass, or sand), and incipient insulation failure. Detecting HIFs on distribution systems with voltage levels below 35 kV is a challenge because the fault currents generated are below the traditional overcurrent element pickup levels. Overcurrent protection based on fundamental or rms quantities of the current is ineffective in detecting HIFs.

8.2.1 HIF Detection

The HIF detection method consists of two main algorithms:

1. HIF1 that uses the odd-harmonic content in the phase currents.
2. HIF2 that uses the interharmonics content in the phase currents.

The following are the key characteristics of the HIF detection algorithms:

- An informative quantity (e.g., the interharmonics content of the phase currents) that reveals the HIF signature without being affected by noise generated by load or switching operations on the system.

- A stable prefault reference established through an initial 24-hour tuning process and updated during normal operation.
- An adaptive tuning function that learns the margin above the reference.
- An effective decision logic to detect HIFs and discriminate HIFs from other system conditions.

The recloser control used in this test uses the HIF2 (nonharmonic) algorithm for fault detection. The block diagram describing HIF detection is shown in Figure 8.5.

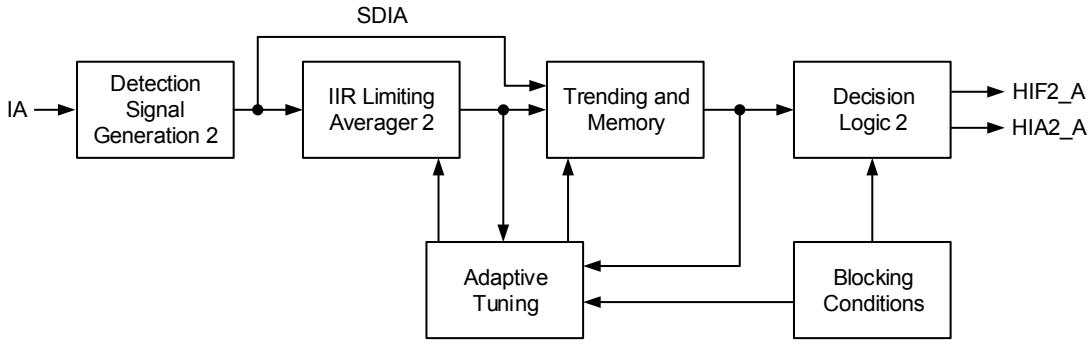


Figure 8.5: Block Diagram of HIF Detection in Recloser Control

The HIF detection element derives an SDI that represents a total nonharmonic content of the phase current to detect an HIF signature. An IIR averaging filter generates a stable reference of SDI (SDI_REF) and adapts to the ambient conditions of the feeder loads. The adaptive tuning function monitors the feeder background noise and determines the margin (d), which is used to identify HIF events. This margin also limits the input to the averager to prevent the reference from following large SDI spikes. The trending and memory function provides information to decision logic about how often (dt) and by how much (rd) SDI departs from SDI_REF, plus the learned margin d. The counting parameters are shown in Figure 8.6.

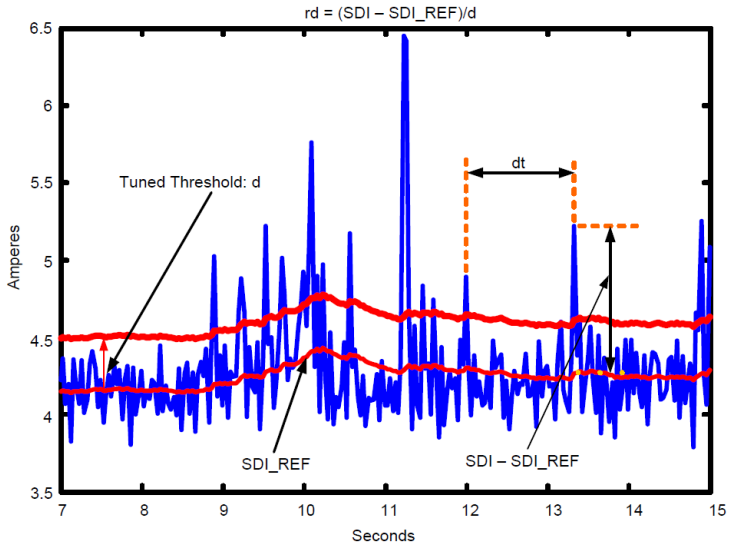


Figure 8.6: HIF2 Algorithm Counting Parameters

The decision logic uses the output from the trending and memory block to determine the existence of an HIF. It has separate counters for HIFs and alarms. Figure 8.7 shows the rd-dt plane that is divided into three regions: Fault Count, Alarm Count, and No Count. The quantity of deviation of SDI from SDI_REF is represented by rd. The

frequency of deviation of SDI from SDI_REF is represented by dt. The dt axis reflects the units of the algorithm processing rate, or the interval over which SDI accumulates.

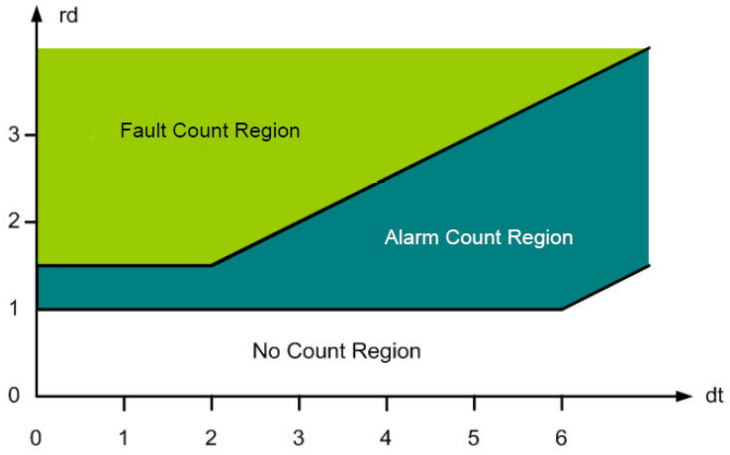


Figure 8.7: HIF2 Algorithm Counting Regions

The counting scheme used here can be correlated to a differential current operating characteristic, where rd is the operating quantity and dt is the restraint quantity. Large dt values coming from sporadic and isolated events, such as lightning or capacitor bank switching, are likely to be disregarded. Conversely, arcing events from HIFs tend to produce high SDI values occurring within a short period; therefore, the corresponding (rd, dt) pairs are more likely to be in the Fault Count region.

If the (rd, dt) pair falls within the No Count region, the algorithm generates no counts for HIFs or alarms. The No Count region accounts for system noise and disturbances generated during the normal power flow. If the pair falls in the Alarm Count region, the algorithm generates counts for alarms only. If the pair falls in the Fault Count region, the algorithm generates counts for both HIFs and alarms.

8.3 TEST PROCEDURE

The following are the steps involved in testing HIFs using the recloser control.

Step 1. Receive the settings from SDG&E for the specific recloser to be tested and load settings to the recloser control.

Step 2. Select Group 1 as the active group for testing purposes and load test settings to Group 1.

Step 3. Set the group setting, EHIF, to T.

Step 4. Set the HIF report setting, HIFLER, to 2 minutes (recommended).

Step 5. Add the HIF2 algorithm Relay Word bits to the SER.

Step 6. Depending on whether the HIF needs to trip the relay or not, set the Trip equation to contain the HIF FAULT bits or set to 0. All other tripping functions, such as switch onto fault (SOTF), are set to 0.

Step 7. Connect the three-phase voltages (V1, V2, and V3) and three-phase currents (I1, I2, and I3). Both will be sent as low-level signals to the recloser control for testing, from the RTDS to the relay via the GTAO card as shown in Figure 8.8. Channels 1 through 3 are reserved for the phase voltages and Channels 4 through 6 are reserved for phase currents. The recloser control has two sets of voltage and current inputs. Therefore, the connections must be made to the active voltage and current source windings.

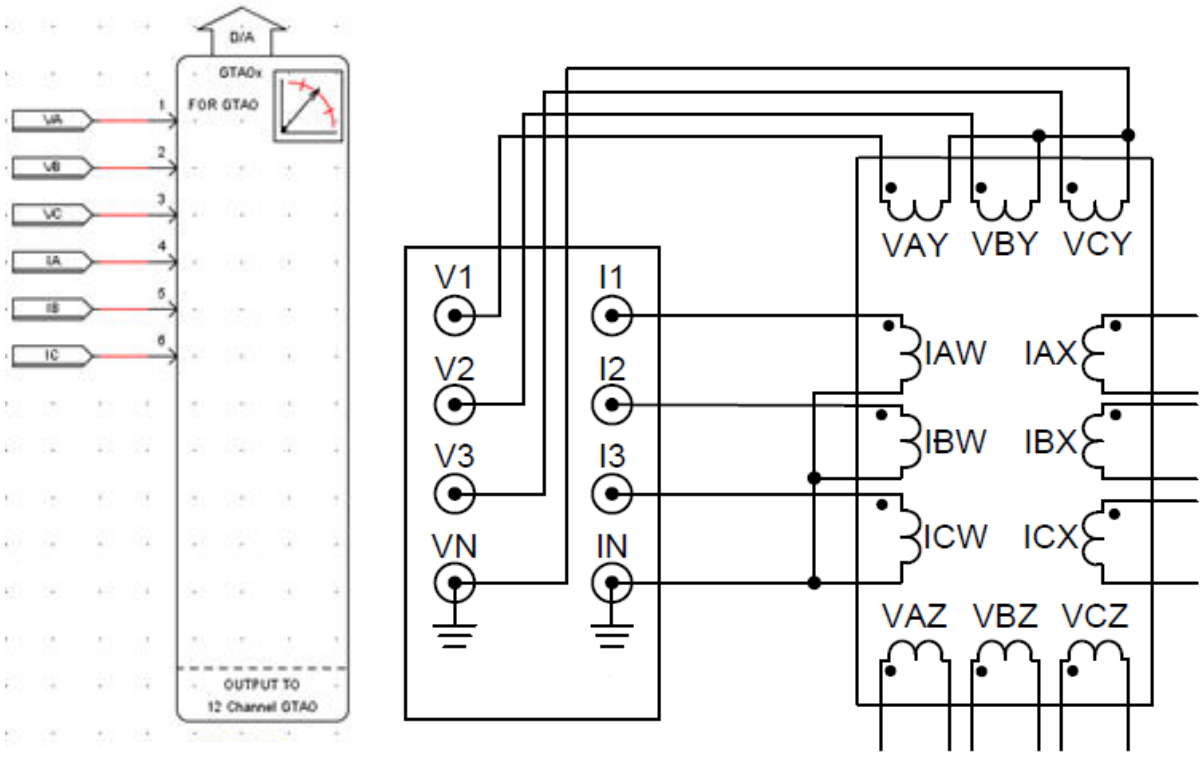


Figure 8.8: Test Setup

Step 8. Apply a balanced three-phase voltage and current. Perform a meter test (MET command) to verify the connections.

Step 9. Issue the STA C command before the start of every test to turn on the relay and reset any dropout timers and latches associated with the high-impedance algorithm.

Step 10. Issue the HIS HIF CA command to clear the HIF event history.

Step 11. Issue the SER C command to clear the SER.

Step 12. Run the test circuit on RTDS and apply high-impedance faults (different fault impedances and fault locations) to test HIF detection.

Step 13. After the test has finished, verify that the HIF2 algorithm outputs associated with the fault have picked up for the phase, or phases, under test.

Step 14. Retrieve the HIF event reports if generated during the test. Also, the RTDS RunTime plots are to be retrieved for each event.

Step 15. Analyze the SER and the event reports.

8.4 RECLOSER CONTROL SETTINGS

The recloser control was set based on the standards specified by SDG&E. The following are the important device settings pertaining to the HIF detection tests.

CTR = 1000

PTR = 266.70

Phase instantaneous overcurrent elements:

50P1P (Level 1 pickup) = 1.0 A secondary

50P1D (pickup delay) = 3.0 cycles

50P2P (Level 2 pickup) = 1.0 A secondary

50P2D (pickup delay) = 0 cycles

Ground instantaneous overcurrent elements:

50G1P (Level 1 pickup) = 1.0 A secondary

50G1D (pickup delay) = 3.0 cycles

50G2P (Level 2 pickup) = 1.0 A secondary

50G2D (pickup delay) = 0 cycles

Ground time-overcurrent elements:

51G1JP (Element J pickup) = 0.1 A secondary

51PJC (Level 1 curve) = U1

51G1JTD (time dial) = 1.0

HIF detection settings:

EHF (HIZ enable) = T (Test mode)

50GHIZP (50GHIZ overcurrent element pickup) = 0.025 A secondary

NPUDO (50GHIZ element pickup/dropoff counts) = 15

TPUDO (NPUDO time window) = 20.0 seconds

NHIZ (HIZ Counts) = 1

THIZ (NHIZ time window) = 120 seconds

The detailed settings for the recloser control were provided by SDG&E and are included in Appendix D.

50GHIZP is the ground HIF detection pickup. When the ground current, IG, is greater than 50GHIZP, element 50GHIZ asserts. When 50GHIZ asserts and deasserts in succession, the NPUDO counter starts recording and the TPUDO timer begins clocking. If the counts threshold is met (15 counts) within the TPUDO window (20 seconds), then another counter, NHIZ, begins. If NHIZ (1 count) is met within THIZ window (120 seconds), then the HIF2_A element will assert and trigger a high-impedance fault. Two counters provide additional security against nuisance tripping.

8.5 TEST SCENARIOS

8.5.1 Auto and Remote Toggle – From Local Control

Table 8.3 illustrates the Auto and Remote Toggle on the Recloser Control.

Table 8.3: Auto and Remote Toggle – Local Control

Objective: Verify appropriate indication for AUTO/REMOTE operating mode.					
Specific instruction: AUTO/REMOTE toggle allowed by **AUTO** and **REMOTE** pushbuttons in LOCAL mode. Carry out Test Action 1, observe corresponding results. Move on to Test Action 2.					
Negative test: Modes do not switch between LOCAL/MANUAL and AUTO/REMOTE.					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. Recloser control in MANUAL mode. **MANUAL** LED is ON.	1. Press **AUTO/MANUAL** pushbutton. 2. Press **AUTO/MANUAL** pushbutton.	1.a. **AUTO** LED – ON 1.b. **MANUAL** LED – OFF 1.c. Recloser control in AUTO mode 2.a. **AUTO** LED – OFF 2.b. **MANUAL** LED – ON 2.c. Recloser control in MANUAL mode.	1. Recloser control switches to AUTO mode successfully. 2. Recloser control switches to MANUAL mode successfully.	Y	
1. Recloser control in MANUAL mode. **MANUAL** LED is ON.	1. Press **REMOTE/LOCAL** pushbutton. 2. Press **REMOTE/LOCAL** pushbutton.	1.a. **REMOTE** LED – ON 1.b. **LOCAL** LED – OFF 1.c. Recloser control in REMOTE mode 2.a. **REMOTE** LED – OFF 2.b. **LOCAL** LED – ON 2.c. Recloser control in LOCAL mode	1. Recloser control switches to REMOTE mode successfully. 2. Recloser control switches to LOCAL mode successfully.	Y	
Test notes: The recloser control may be placed in Automatic mode when there are no lockout conditions and all three-phase voltages are healthy. Observe system voltage profile after switching operation.					

8.5.2 High-Impedance Fault Detection

HIF detection is performed by the recloser control based on the settings recommended by SDG&E. An HIF creates fault currents that fall well below the overcurrent pickup values; however, they persist long enough to possibly damage the system components. The recloser control detects these fault currents based on its HIF logic.

Scenario 1

Scenario 1 describes the HIZ element overcurrent pickup, as shown in Table 8.4.

Table 8.4: 50GHIZ Overcurrent Pickup Element Test

Objective: Verify the high-impedance overcurrent element (50GHIZ) picks up for HIFs.					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. System with nominal voltage and current conditions. 2. HIZ fault detection enabled.	1. Apply an HIF of 85 ohms for 200 ms close in to the recloser.	1.a. The 50GHIZ high-impedance overcurrent fault element asserts. 1.b. No other overcurrent elements assert.	The 50GHIZ element asserts as desired when the fault current crosses the element threshold.	Y	
Test notes:					

Figure 8.9, Figure 8.10, and Figure 8.11 illustrate an HIF generated close in to the recloser. Figure 8.9 is the event report of the fault as seen by the recloser control. As shown, the 50GHIZ element picks up when the fault is initiated; however, no other protection elements pick up because the fault does not cross their respective thresholds. Figure 8.10 shows that only one spike is captured because the HIF is not recurring. Figure 8.11 shows the SER for the HIF.

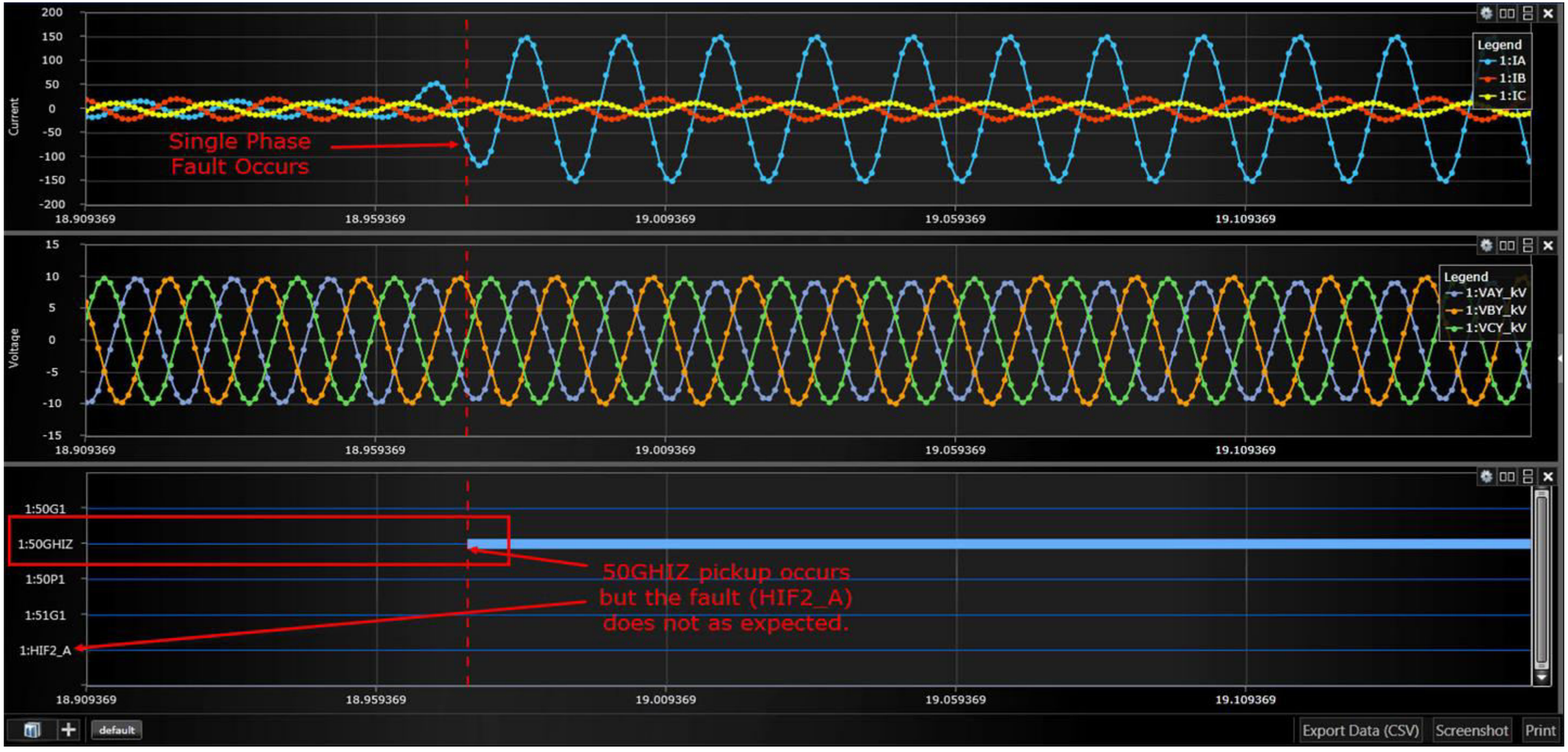


Figure 8.9: Scenario 1 – Event Report – 50GHIZ Pickup

Figure 8.10: Scenario 1 – C1215-32R Current A Magnitude – Single Spike

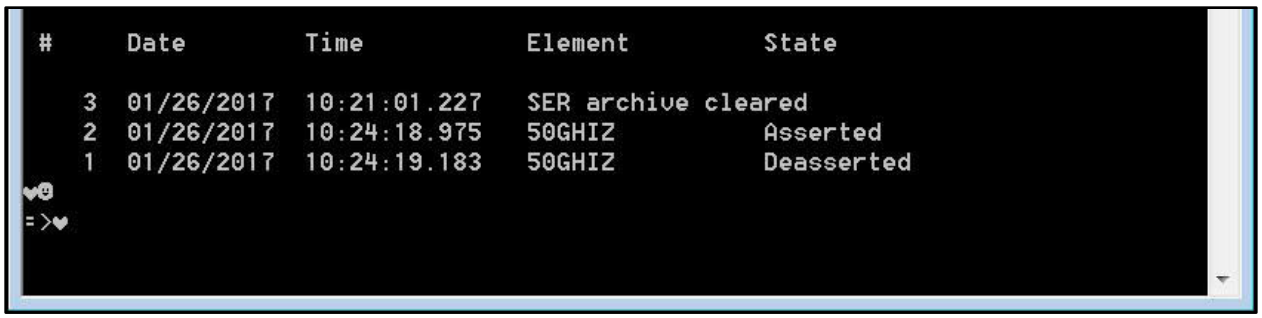


Figure 8.11: Scenario 1 – SER Report – 50GHIZ Pickup

Scenario 2

Table 8.5 illustrates a scenario where HIF is detected by the recloser.

Table 8.5: HIF Detection

Objective: Verify if recloser detects HIFs.					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. System with nominal voltage and current conditions. 2. HIZ fault detection enabled.	1. Apply an HIF of 85 ohms on the A phase that persists for a duration of 200 ms. Repeat 15 times within 20 s.	1.a. The 50GHIZ high-impedance overcurrent fault element asserts. 1.b. The A phase HIF2_A element asserts to indicate a high-impedance fault. 1.c. No other overcurrent elements assert.	The 50GHIZ element asserts. After 15 counts of the element, the HIF2_A element asserts, indicating a high-impedance fault.	Y	
Test notes:					

This test was carried out for increasing values of impedance until a point when the impedance triggered an HIF element and no other protection element. It was observed that for faults below 85 ohms, the 50G and 51G elements triggered, indicating a normal single-line-to-ground fault, which is illustrated in Scenario 4. Figure 8.12, Figure 8.13, and Figure 8.14 illustrate an HIF generated close in to the recloser. Figure 8.12 is the event report of the fault as seen by the recloser control. As shown, the 50GHIZ element picks up when the fault is initiated. The 50GHIZ element picks up and drops off for 15 counts resulting in the high-impedance fault element, HIF2_A, asserting. This indicates an HIF on the line. No other protection element asserts for this fault. Figure 8.13 shows that 15 spikes are counted within 20 seconds to meet the HIF2_A criteria. Figure 8.14 shows the SER for the HIF.

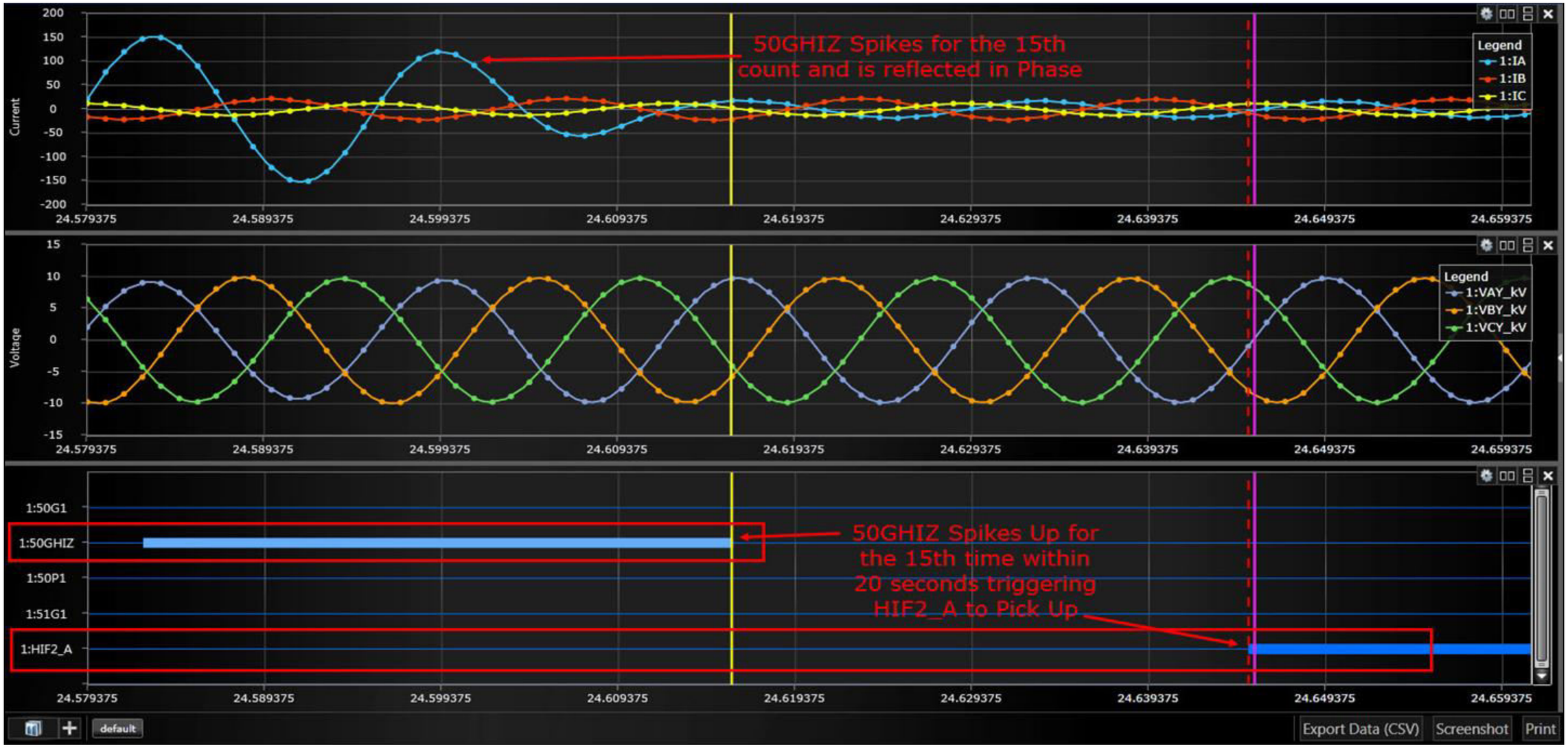
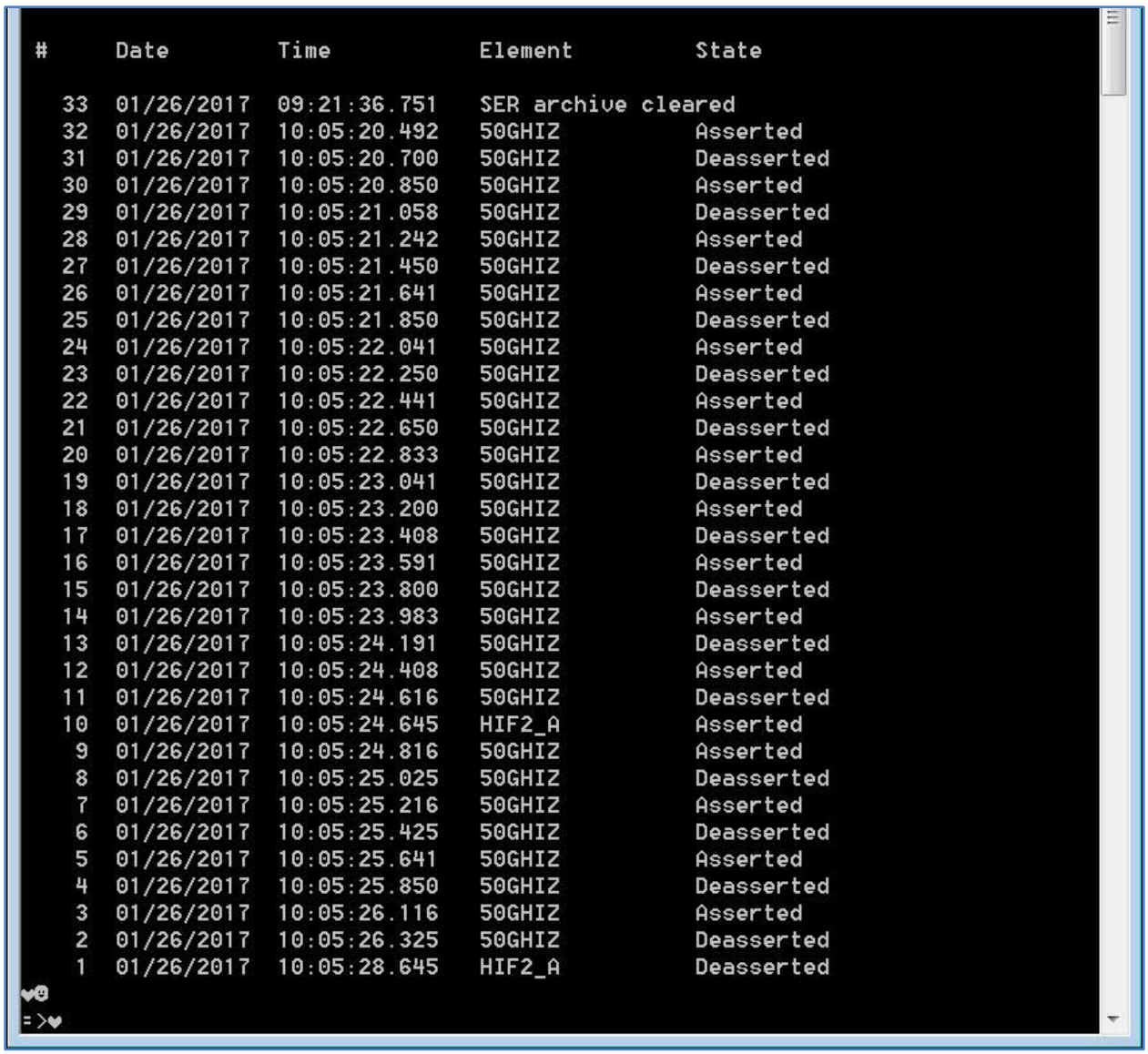


Figure 8.12: Scenario 2 – Event Report – 50GHIZ and HIF2_A Pickup

Figure 8.13: Scenario 2 – Central C1215-32R Pickup



#	Date	Time	Element	State
33	01/26/2017	09:21:36.751	SER archive cleared	
32	01/26/2017	10:05:20.492	50GHIZ	Asserted
31	01/26/2017	10:05:20.700	50GHIZ	Deasserted
30	01/26/2017	10:05:20.850	50GHIZ	Asserted
29	01/26/2017	10:05:21.058	50GHIZ	Deasserted
28	01/26/2017	10:05:21.242	50GHIZ	Asserted
27	01/26/2017	10:05:21.450	50GHIZ	Deasserted
26	01/26/2017	10:05:21.641	50GHIZ	Asserted
25	01/26/2017	10:05:21.850	50GHIZ	Deasserted
24	01/26/2017	10:05:22.041	50GHIZ	Asserted
23	01/26/2017	10:05:22.250	50GHIZ	Deasserted
22	01/26/2017	10:05:22.441	50GHIZ	Asserted
21	01/26/2017	10:05:22.650	50GHIZ	Deasserted
20	01/26/2017	10:05:22.833	50GHIZ	Asserted
19	01/26/2017	10:05:23.041	50GHIZ	Deasserted
18	01/26/2017	10:05:23.200	50GHIZ	Asserted
17	01/26/2017	10:05:23.408	50GHIZ	Deasserted
16	01/26/2017	10:05:23.591	50GHIZ	Asserted
15	01/26/2017	10:05:23.800	50GHIZ	Deasserted
14	01/26/2017	10:05:23.983	50GHIZ	Asserted
13	01/26/2017	10:05:24.191	50GHIZ	Deasserted
12	01/26/2017	10:05:24.408	50GHIZ	Asserted
11	01/26/2017	10:05:24.616	50GHIZ	Deasserted
10	01/26/2017	10:05:24.645	HIF2_A	Asserted
9	01/26/2017	10:05:24.816	50GHIZ	Asserted
8	01/26/2017	10:05:25.025	50GHIZ	Deasserted
7	01/26/2017	10:05:25.216	50GHIZ	Asserted
6	01/26/2017	10:05:25.425	50GHIZ	Deasserted
5	01/26/2017	10:05:25.641	50GHIZ	Asserted
4	01/26/2017	10:05:25.850	50GHIZ	Deasserted
3	01/26/2017	10:05:26.116	50GHIZ	Asserted
2	01/26/2017	10:05:26.325	50GHIZ	Deasserted
1	01/26/2017	10:05:28.645	HIF2_A	Deasserted

Figure 8.14: Scenario 2 – SER Report – 50GHIZ Picks Up 15 Times to Trigger HIF2_A

Scenario 3

Scenario 3 involves running the 24-hour load profile and observing the recloser operation for the duration. The test is described in Table 8.6.

Table 8.6: Recloser Response During Load Profile Operation

Objective: Verify if the recloser HIF logic operates during a normal load profile.					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. System with nominal voltage and current conditions. 2. Run the system in the normal load profile. 3. HIZ fault detection enabled.	1. Run the system in the normal load profile and observe recloser operation, if any.	1. The 50GHIZ or the HIF2_A, HIF2_B, or HIF2_C do not operate.	The 50GHIZ or the HIF elements do not operate.	Y	
Test notes:					

Figure 8.15 and Figure 8.16 illustrate the visualization software and the SER report for the duration of the normal load profile operation. As observed from the SER log in Figure 8.16, none of the HIF elements operate from the start to the end of the 24 hour load profile run. This is the desired result for a normal operation of the system.

Figure 8.15: Scenario 3 – Central with 24-Hour Load Profile

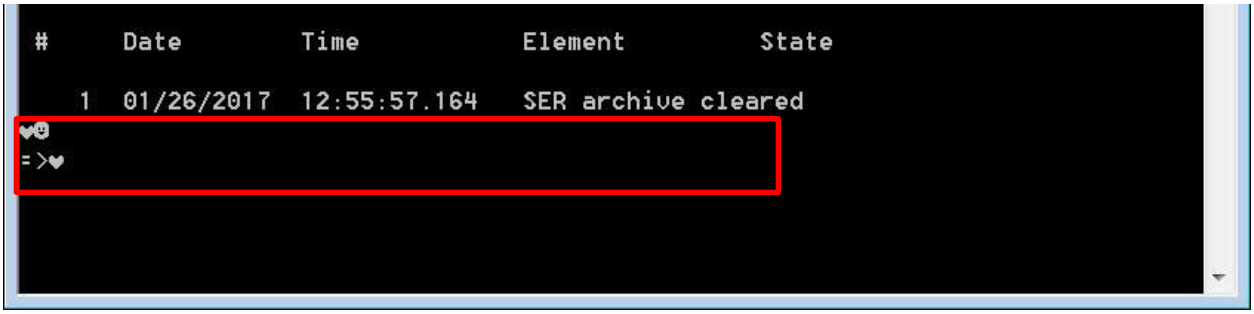


Figure 8.16: Scenario 3 – SER Shows No Pickup on a 24-Hour Load Profile Cycle as Expected

Scenario 4

Scenario 4 involves observing the recloser operation for a bolted fault. Table 8.7 describes this scenario.

Table 8.7: Recloser Operation During Bolted Fault

Objective: Verify recloser operation for a bolted fault.					
Test Initial Conditions	**Test Actions**	**Expected Results**	**Actual Results**	**Pass**	**Fail**
1. System with nominal voltage and current conditions. 2. HIZ fault detection enabled.	1. Apply a bolted fault on the A phase.	1.a. The 50 and 51 overcurrent ground elements assert, indicating a phase-to-ground fault. 1.b. The 50GHIZ asserts. 1.c. The HIF2_A element does not assert because the fault does not satisfy the spike count requirements.	1. The 50G1, 51G1 and 50P1 elements assert. 2. The 50GHIZ element asserts, but HIF2_A element does not assert.	Y	
Test notes:					

Figure 8.17, Figure 8.18, and Figure 8.19 illustrate the visualization software and the SER report for a bolted fault to assure the HIF2_A element does not pick up. The HIF2_A high-impedance fault element does not operate during the bolted fault (see elements in Figure 8.17 and Figure 8.19), which is desired.

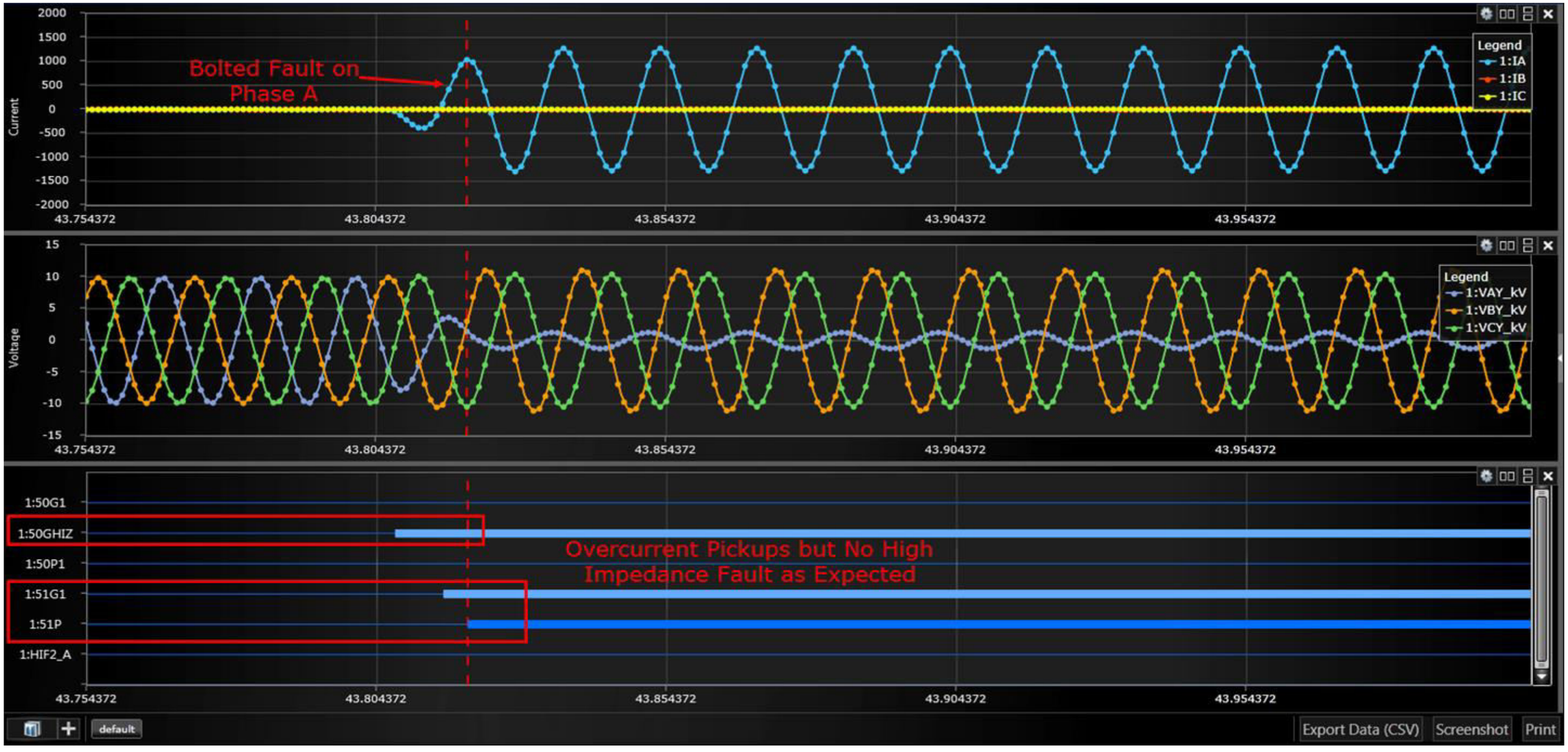


Figure 8.17: Scenario 4 – Overcurrent Protection Pickups with No HIF Pickup

Figure 8.18: Scenario 4 – Central Single Spike Does Not Meet HIF Criteria

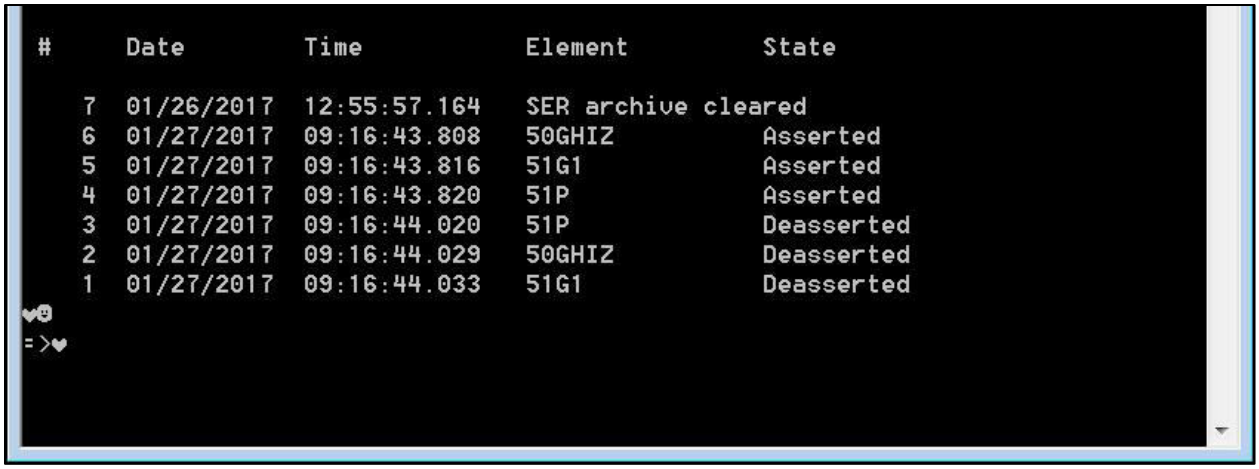


Figure 8.19: Scenario 4 – SER Shows Expected Overcurrent Pickups

8.6 RECOMMENDATION

It is recommended that SDG&E monitor the coastal-residential, urban, and desert-rural test circuits carefully for HIFs. The tests show that the high-impedance protection works as expected and can be used to indicate how the SDG&E circuits will behave in the event of an HIF. It is recommended to monitor the circuit operations closely to fine tune the HIF detection settings for each circuit. For reclosers in the field, it is recommended to look at field data and formulate HIF settings based on the circuit behavior and characteristics.

9 POWER QUALITY IN ISLANDS

The objective of this test was to define different system island configurations and observe voltage and frequency on pre- and post-islanded systems. PMUs were placed along the length of the desert-rural circuit in RSCAD to record these parameters. These tests demonstrate how synchrophasors can be applied to monitor voltage, frequency and any other relevant circuit parameters, real-time, during switching in and out of an island. The information obtained can be used to set up accurate protection and control parameters to maintain frequency and voltage in band during switching.

9.1 ISLAND CONFIGURATIONS

The desert-rural test circuit is selected for the demonstration of these tests. Three island configurations are considered for this purpose.

Island 1: This island is formed when Way 1 of the switch (D149479) is opened. Loads LD1 and LD2 are a part of the island supported by DER D149478 rated at 12 kV, 1000 kW. The rest of the circuit is supported by the utility. Refer to Figure 9.1.

Island 2: This island is formed when the normally-closed recloser 1215-10R is opened. Loads LD1, LD2, and LD3 are a part of the island supported by DER D149478 rated at 12 kV, 1000 kW. The rest of the circuit downstream of 1215-12R is supported by the utility. Refer to Figure 9.2.

Island 3: This island is formed when the substation feeder breaker is open and the utility source is unavailable. The entire test circuit is supported by DER D149478. Refer to Figure 9.3. Island 3 is considered for test demonstrations in this report.

The generation capacity of the DER may have to be adjusted via the slider in RTDS RunTime to meet the load requirement for all three island configurations. The island tests were carried out based on the 24-hour load profile for the test circuit.

Note: Refer to Table 9.1 for load distribution across the desert-rural Circuit C1215.

Table 9.1: Desert-Rural Test Circuit – Load Distribution

RTDS/Visio Reference	kW – A	kW – B	kW – C	KVAR – A	KVAR – B	KVAR – C
LD1	113	102	116	37	33	38
LD2	399	385	427	132	125	141
LD3	14	19	72	5	6	24
LD4	0	25	0	0	8	0
LD5	0	0	20	0	0	7
LD6	9	51	15	3	16	5
LD7	55	80	35	19	26	11
LD8	6	21	27	2	6	9
LD9	0	53	18	0	19	6
LD10	124	0	0	39	0	0
Total Load	720	736	730	237	239	241

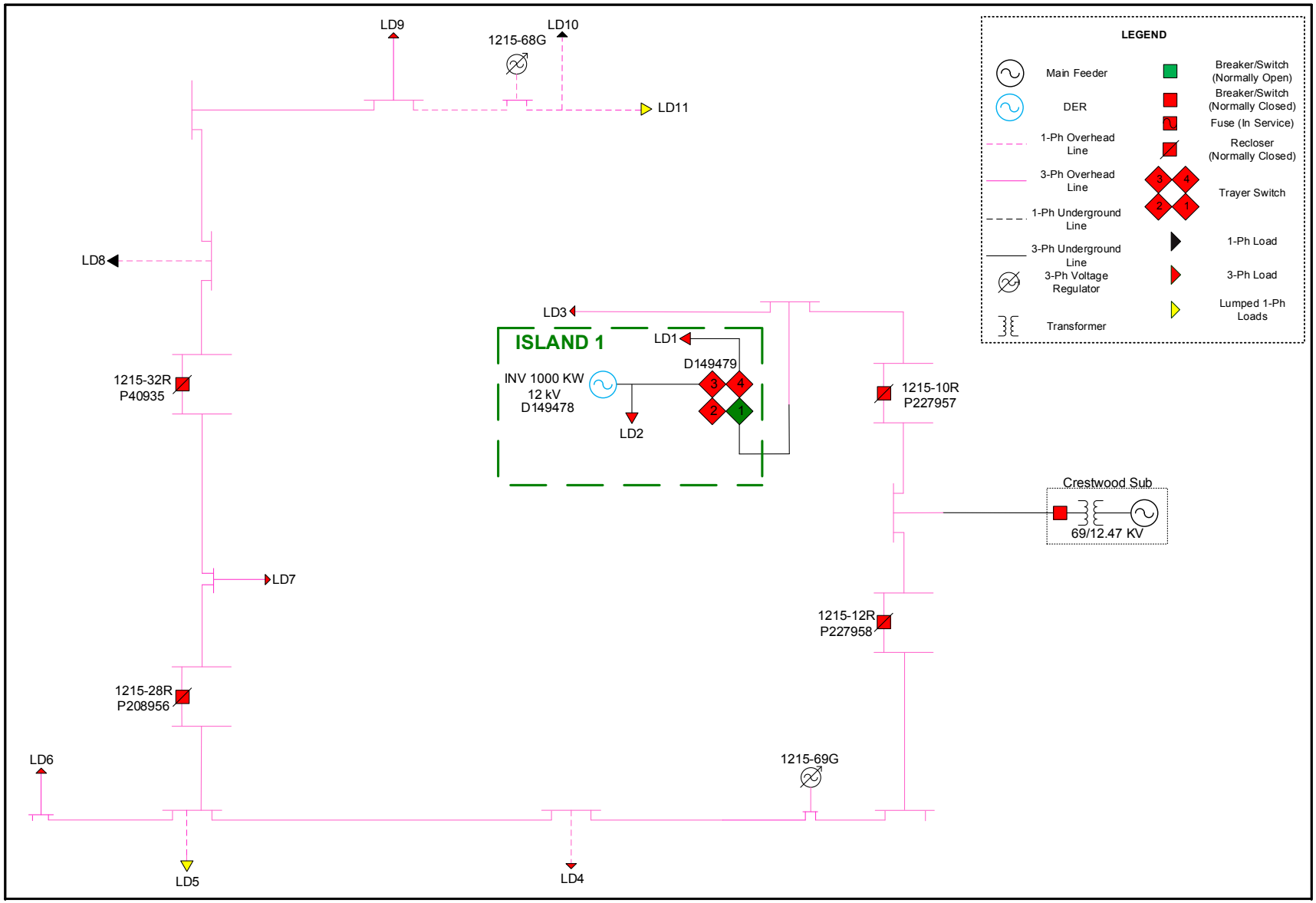


Figure 9.1: Desert-Rural Test Circuit – Island 1

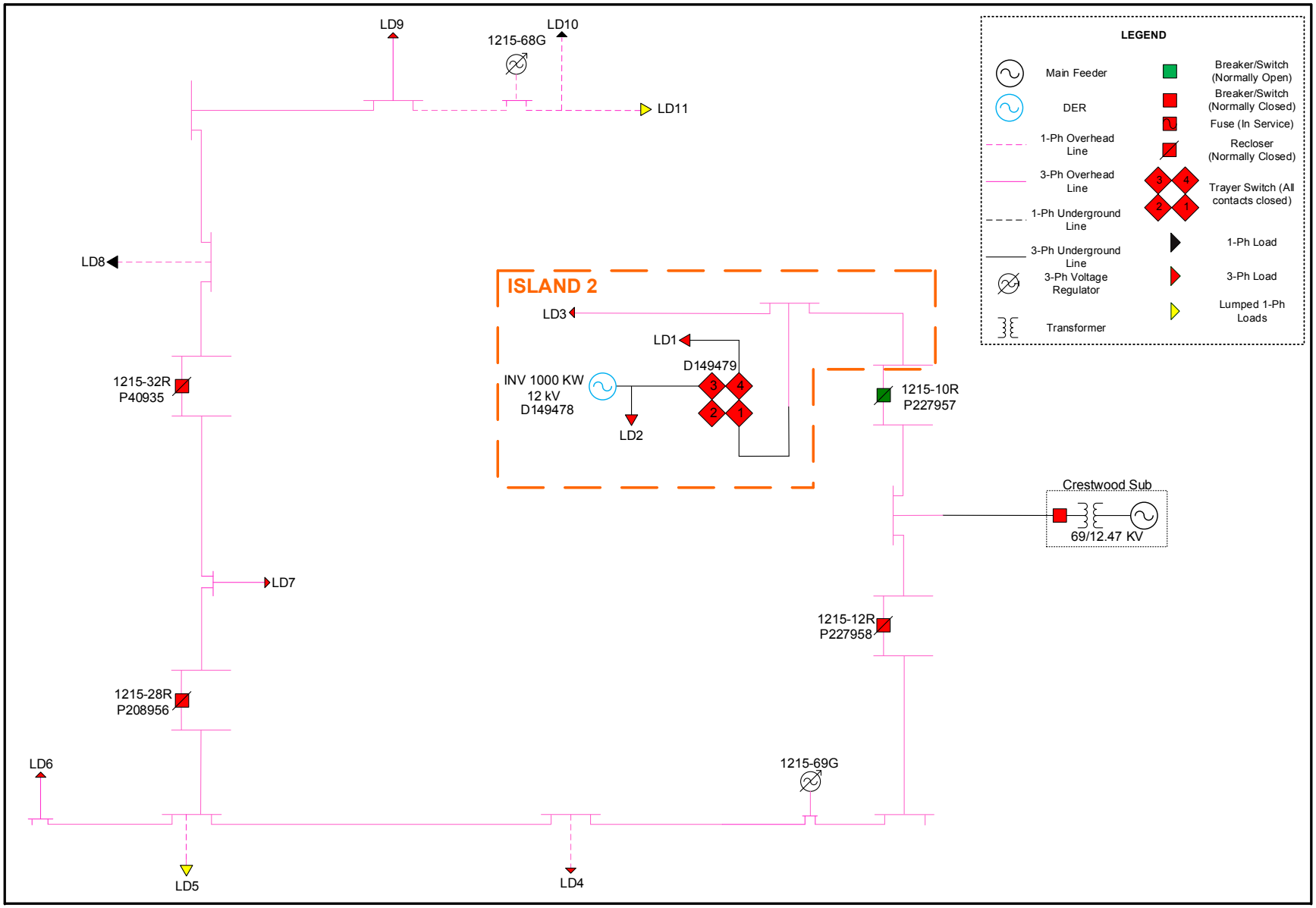


Figure 9.2: Desert-Rural Test Circuit – Island 2

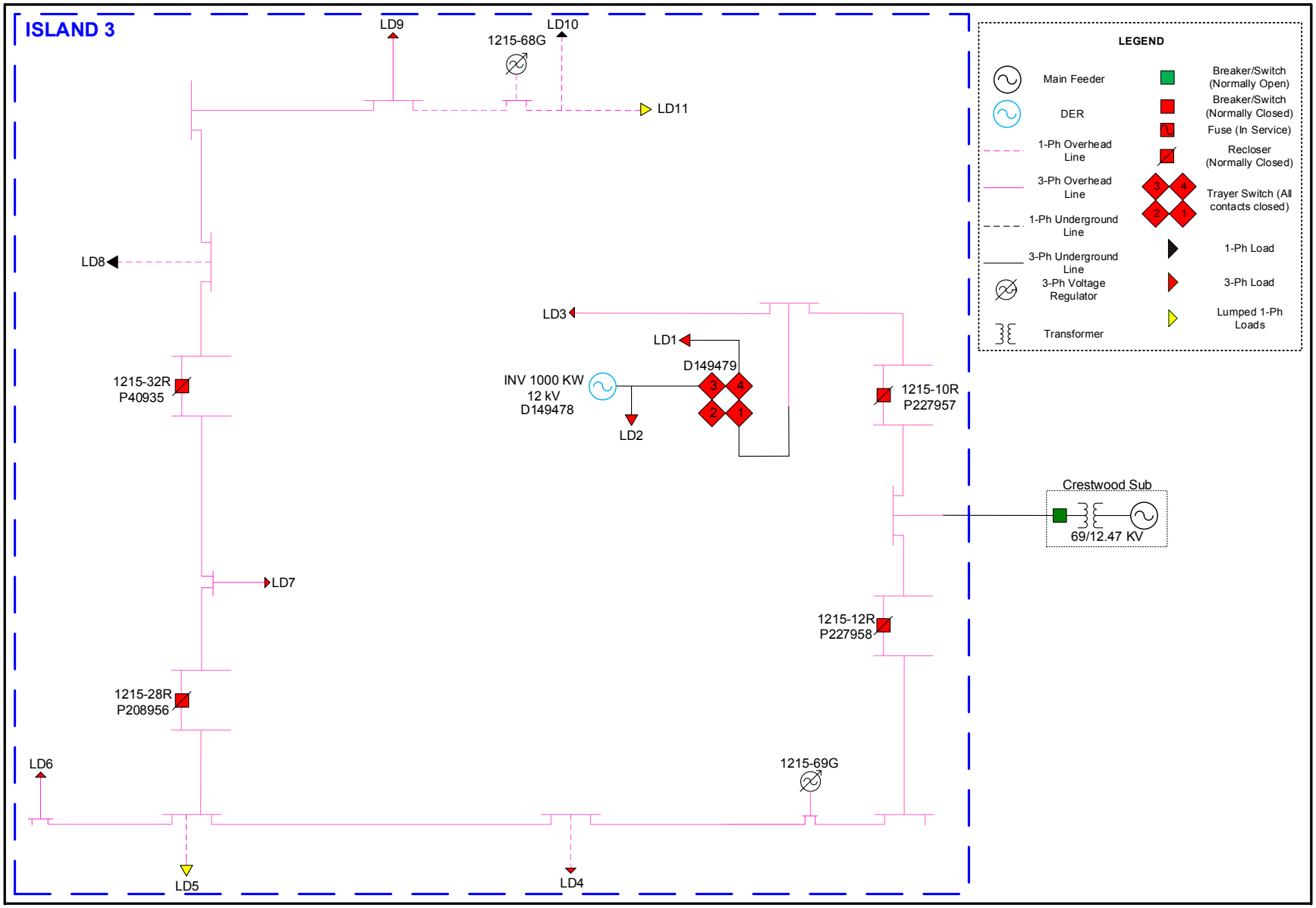


Figure 9.3: Desert-Rural Test Circuit – Island 3

9.2 TEST SETUP

9.2.1 Phasor Measurement Units

Software PMUs are modeled in RSCAD at Locations 1 through 4 for these tests. Location 5 is represented by a hardware PMU and a power quality meter to record harmonics. Refer to Figure 9.4 for more details.

The PMUs are placed such that synchrophasor data over the entire length of the circuit can be collected and analyzed.

1. Location 1: At DER to monitor the parameters at the source level. It is referred to as L1 on the visualization software results screen.

2. Location 2: At D149479 that marks the end of the circuit for Island 1 (Island 3 is studied based on the tests described in this document). It is referred to as L2 on the visualization software results screen.

3. Location 3: At Voltage Regulator 1215-69G as an intermediate point on the circuit. It is referred to as L3 on the visualization software results screen.

4. Location 4: At Recloser 1215-32R as an intermediate point on the circuit. It is referred to as L4 on the visualization software results screen.

5. Location 5: At load LD10 to collect data from the end of the circuit. It is referred to as L5 on the visualization software results screen.

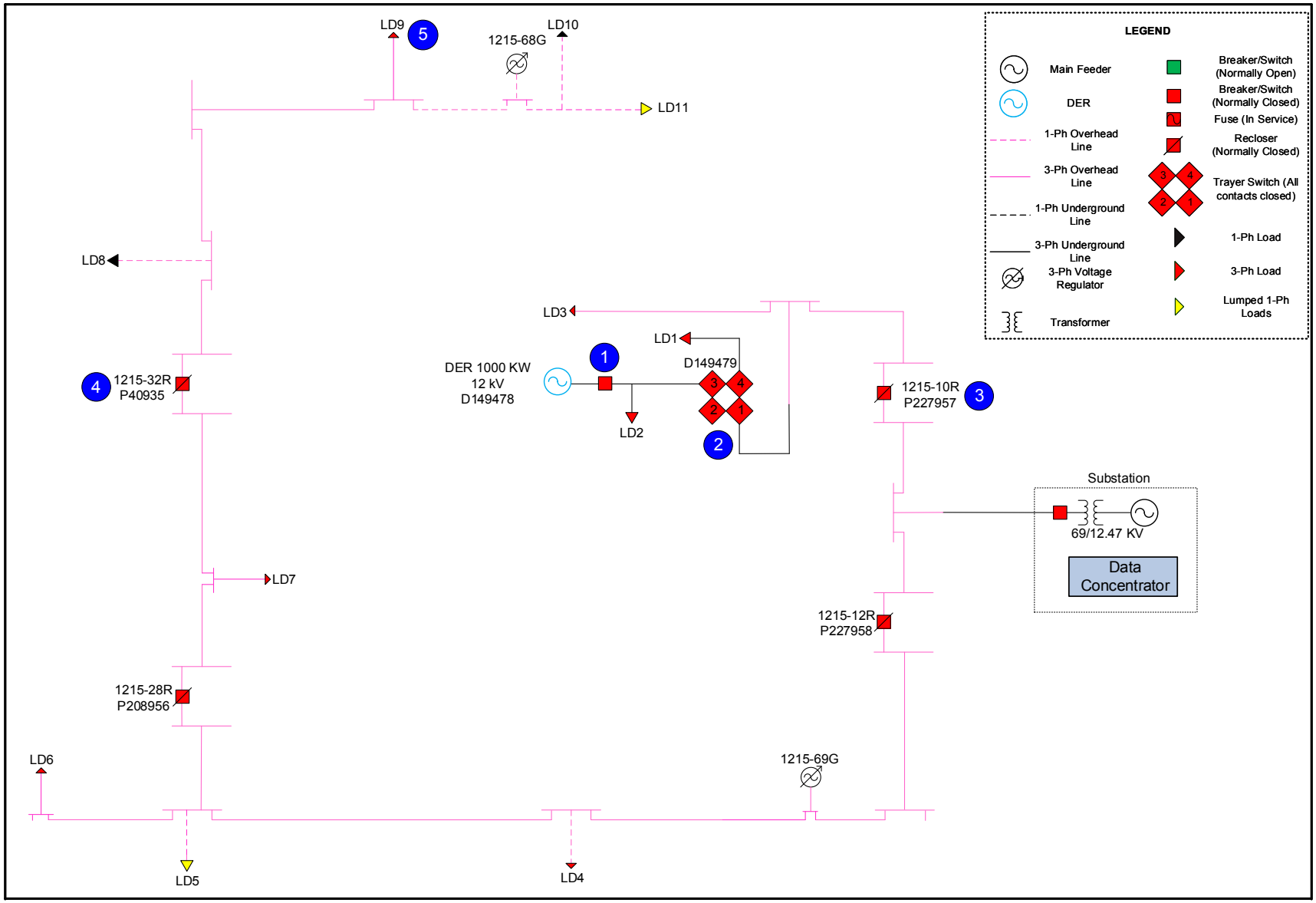


Figure 9.4: Locations of PMUs

9.2.2 RTDS and PMU Interface

Figure 9.5 illustrates the interface between the RTDS and the hardware PMU. The power quality meter is connected to the RTDS I/O cube such that it receives analog and digital inputs from the RTDS. The meter has a low-level test interface available and therefore no amplifiers are required between the RTDS and the meter for analogs.

The software PMUs are modeled in RSCAD software.

Note: ABC phase rotation is considered.

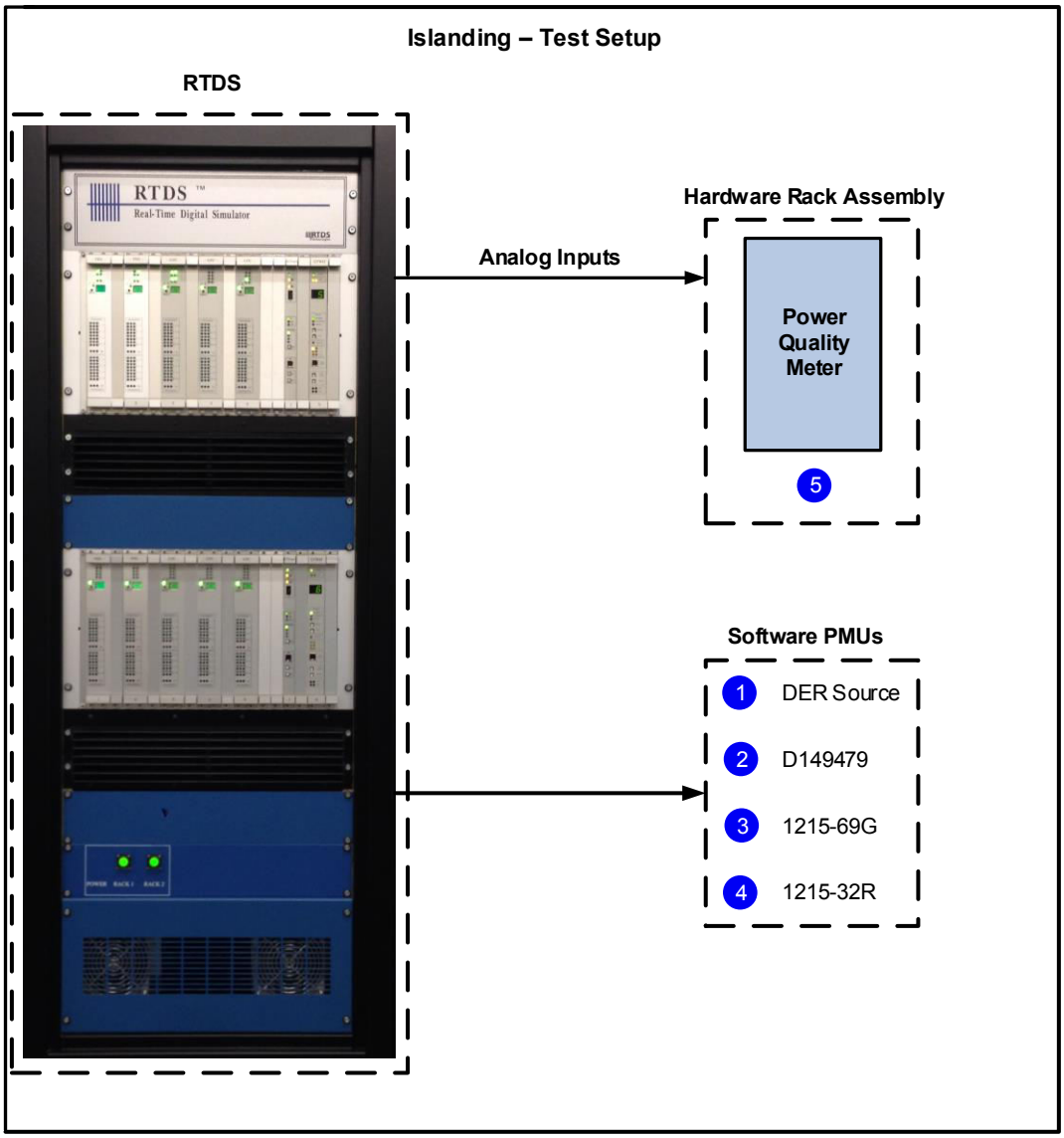


Figure 9.5: RTDS and PMUs Interface

9.2.3 PMU Communications Architecture

In addition to the PMU locations discussed in the previous section, the data concentrator is considered at the substation level. The data concentrator collects phasor, analog, and digital data over synchrophasor protocol (conforming to IEEE C37.118.1-2011) from the field PMUs.

Figure 9.6 shows the configuration required to establish successful communication between the PMUs and data concentrator over synchrophasor protocol. The PMUs and data concentrator are connected to an unmanaged Ethernet switch so that all devices are on the same network. A satellite-synchronized clock is used to provide an IRIG-B signal to all PMUs for time synchronization. A test computer to configure the PMU and the data concentrator settings is also added in the same network.

Time-aligned phasor data collected from all field PMUs is displayed collectively on one platform for further analysis using a visualization software.

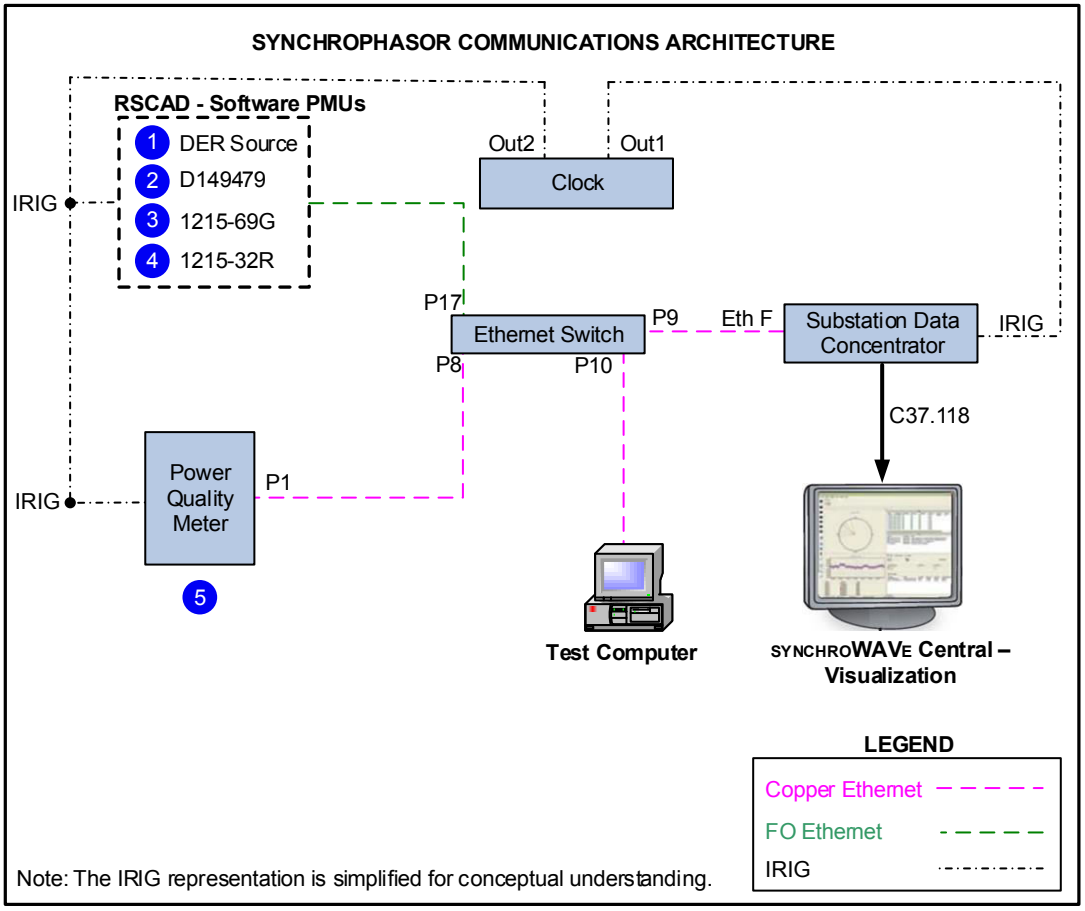


Figure 9.6: Synchrophasor Communications Architecture

9.3 TEST PROCEDURE AND RESULTS

The following tests are performed based on the island configurations discussed in Section 9.1. Test results in the form of voltage phasors and analogs are shown for visualization.

9.3.1 Test 1

Observe the voltage profile along the island and ensure it is within the allowed bands. According to ANSI C84.1-2006, American National Standard for Electric Power Systems and Equipment, the DER island system should be able to actively regulate within the agreed-upon ranges, as specified in Table 9.2 and Table 9.3.

Table 9.2: ANSI C84.1-2006 Standard Nominal System Voltages and Voltages Range – Service Voltage

Nominal Voltage (V)	Service Voltage (V)			
	Range A		Range B	
	Maximum	Minimum	Maximum	Minimum
120	126	114	127	110
240	252	228	254	220
480	504	456	508	440

Table 9.3: ANSI C84.1-2006 Standard Nominal System Voltages and Voltages Range – Utilization Voltage

Nominal Voltage (V)	Utilization Voltage (V)			
	Range A		Range B	
	Maximum	Minimum	Maximum	Minimum
120	125	110 (108)[1]	127	106 (104)[1]
240	250	220 (216)[1]	254	212 (208)[1]
480	500	440 (432)[1]	508	424 (416)[1]

[1] Not applicable to lighting loads.

In Table 9.2 and Table 9.3, Range A refers to the optimal voltage range; whereas, Range B is acceptable, however it is not optimal. In addition, the difference between minimum service and minimum utilization voltages is intended to allow for a voltage drop in the customer wiring. The NEC allows up to a 5 percent drop: up to a 3 percent drop in the main feeder and an additional less than 3 percent drop in individual branch circuits.

Notes:

1. The nominal voltage specified in Table 9.2 and Table 9.3 may need to be scaled for analysis of the 12 kV or 12.47 kV SDG&E circuits.

2. SDG&E will confirm the acceptable voltage band, based on practice.

Results/observations: Figure 9.7 shows the voltage profile at the five locations for the Island 3 scenario as discussed in Section 9.1. Momentary voltage spikes were observed at the time of switching in and out of the island. The voltage profile recovers and steady-state voltages are observed for the rest of the load profile in the island. Additional voltage monitoring and control devices are recommended to dampen these transients quickly to prevent protective relaying in the island from tripping.

Figure 9.7: Voltage Monitoring in Island 3

9.3.2 Test 2

Power quality: Observe THD for currents and voltages, if any.

According to IEEE 1547.4-2011, IEEE Guide for Design, Operation, and Integration of Distributed Resource Island Systems with Electric Power Systems, the DER island system should meet IEEE 519-2014 as shown in Table 9.4 and Table 9.5.

Table 9.4: IEEE 519-2014 Maximum Harmonic Current Distortion in Percent of Current

Individual Harmonic Order h (Odd Harmonics)	h < 11	11 ≤ h < 17	17 ≤ h < 23	23 ≤ h < 35	35 ≤ h	Total Demand Distortion (TDD)
Percentage (%)	4	2	1.5	0.6	0.3	5

Table 9.5: IEEE 519-2014 Maximum Harmonic Voltage Distortion in Percent

Bus Voltage V at Point of Common Coupling	Individual Harmonic (%)	THD (%)
1 kV < V > 69 kV	3	5

Note: Harmonic-related tests are not feasible in the laboratory environment because the DER and the load models do not inject harmonics in the circuit.

9.3.3 Test 3

Observe the frequency pattern before and after island formation. According to IEEE 1547.4-2011, the frequency deviation of a DER island system needs to be acceptable to all associated parties. North American power systems normally operate at 60 Hz with a tight frequency band of ± 0.05 Hz. SDG&E will confirm acceptable frequency bands, based on practice.

Results/observations: Momentary frequency spikes were observed at the time of switching in and out of the island as shown in Figure 9.8 for the Island 3 scenario. The frequency was found to be outside the band of ± 0.05 Hz for the duration of the test in the island scenario. Frequency monitoring and control devices are recommended to control the frequency when in an island scenario to ensure that it stays within the agreed-upon band. The RTDS test case does not include a frequency controller in a feedback loop to maintain the IEEE acceptable frequency band.

These tests demonstrate the application of synchrophasors to gather and analyze data, such as frequency and voltage, at different points in the distribution circuit using PMUs. The data collected over real-time provides a deeper understanding of the system dynamics. This concept can be applied in the field environment where the information obtained can be used to set up accurate protection and control parameters to maintain frequency and voltage in band during switching in and out of an island or any other scenario.

Figure 9.8: Frequency Monitoring in Island 3

10 VOLTAGE SUPPORT COODINATION TESTS

Typically, distribution circuits have a variety of voltage correction devices that regulate the voltage within the specified band. These devices operate in a stand-alone mode depending on the local voltage conditions seen by the voltage correction devices. This section demonstrates a scheme developed to control the switching of multiple voltage correction devices from a central controller.

The objective of these tests is to study the system response and interaction between a DER and a voltage regulator to regulate the voltage profile by meeting the reactive power demand of the system. The switching order of these devices is managed by the algorithm running in a central controller modeled in RSCAD software. Two operating scenarios were defined to validate the scheme. Refer to Section 10.3.1.

10.1 CIRCUIT SELECTION

The desert-rural test circuit is selected for this test. The circuit has a DER and voltage regulators which forms a basic circuit where the interaction between two varied voltage correction devices can be studied. The desert rural circuit with the DER at Position 1 and voltage regulators at Positions 2 and 3 are shown in Figure 10.1.

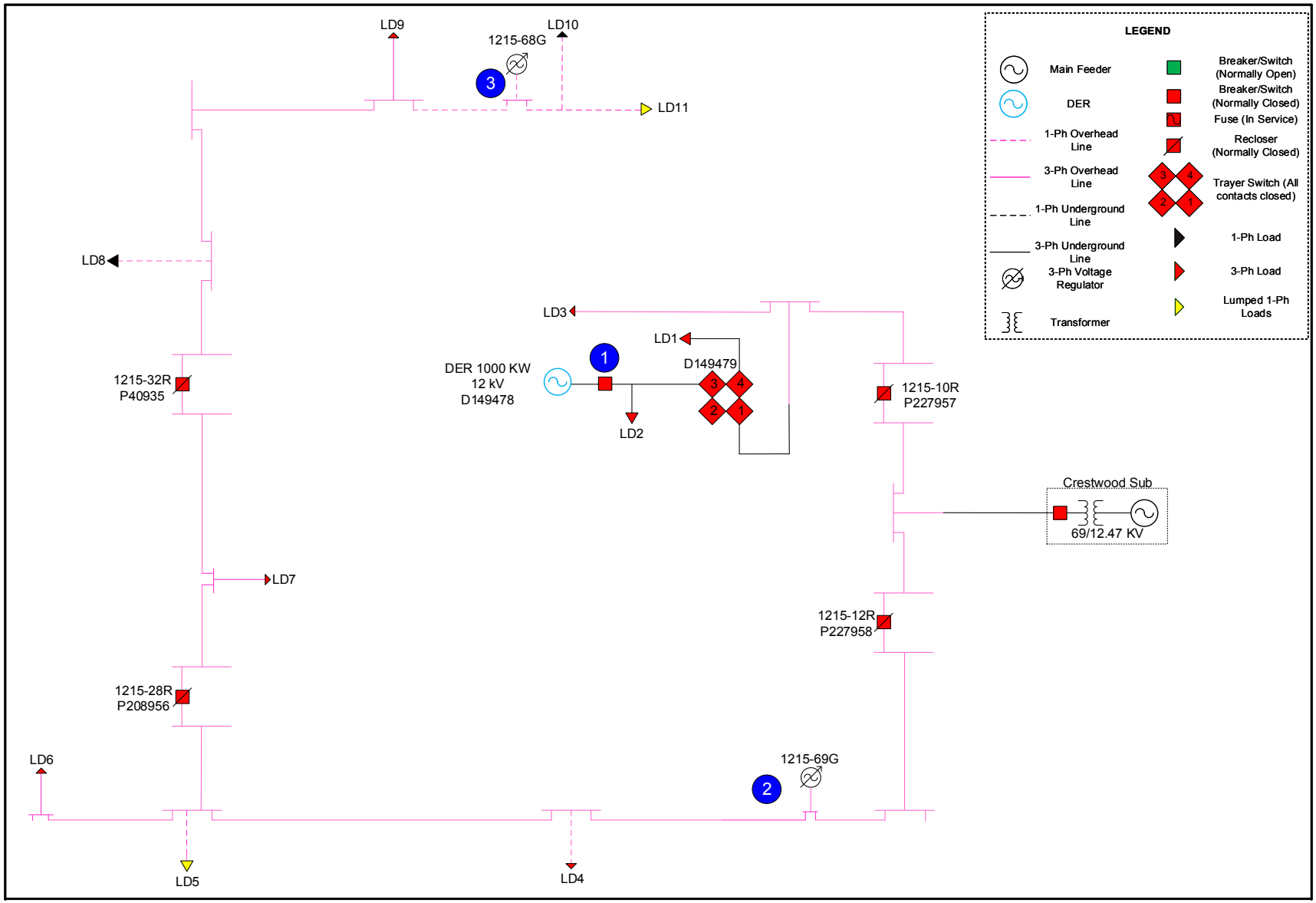


Figure 10.1: Desert-Rural Test Circuit

10.2 TEST SETUP

The desert-rural test circuit with DER and voltage regulators were modeled in RSCAD for this test. This test setup does not include hardware devices. Logic to control and coordinate the DER and voltage regulators is designed in RSCAD. All results are recorded and compiled on the RSCAD RunTime screen.

10.2.1 Distributed Energy Resource

The DER used in these tests have been updated from a scalable constant current source to a scalable battery system that can operate under Volt/VAR mode. The DER battery stacks are controlled by the DER controller. The controller operates in the dq plane with real and reactive power sliders to control the DER output.

The Volt/VAR mode provides smooth control over the reactive power output of the DER in response to the fluctuations in the bus voltage. The bus voltage reference can be set to a desired value in the controller. When the bus voltage goes below this reference, the controller boosts the reactive power output to meet the reactive power deficit of the system. Similarly, it can consume reactive power when the system voltage rises above the reference value. The volt/VAR characteristic is shown in Figure 10.2.

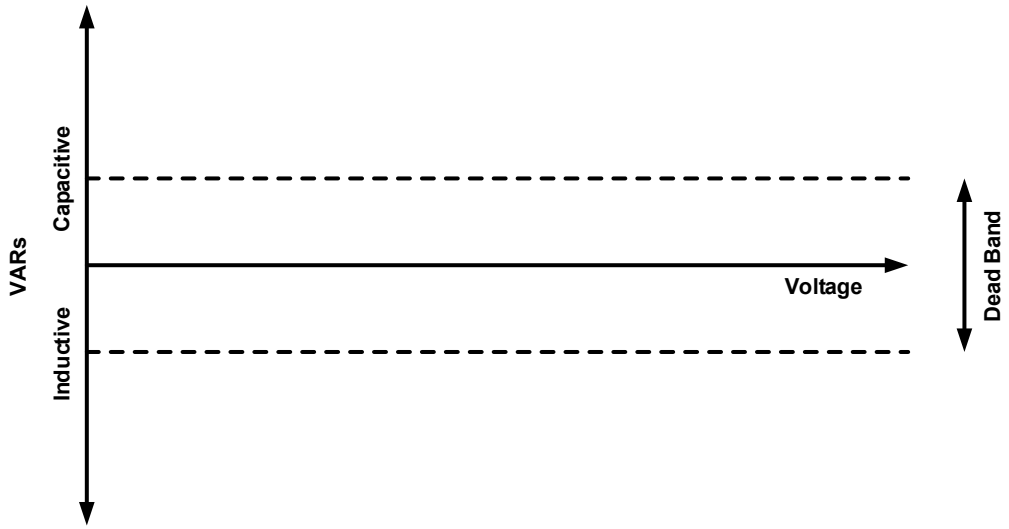


Figure 10.2: Volt/VAR Mode Operation

The DER in the Volt/VAR mode receives the system voltage and monitors the difference against a user-defined reference voltage. Based on the output from the comparator, the volt/VAR controller calculates the increment or decrement to the existing reactive power output using an integral controller. The volt/VAR controller logic is illustrated in Figure 10.3.

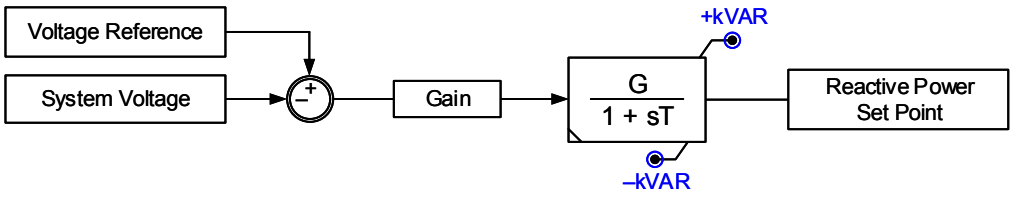


Figure 10.3: Volt/VAR Controller Logic

10.2.2 Voltage Regulator

The voltage regulator logic used in these tests is an extension of the voltage regulator logic described in Section 6.6. Additional logic was added to replicate the hardware connected to the circuit, which is the voltage regulator control. The voltage center band and bandwidth are user defined, which sets the upper and lower voltage band limits of the voltage regulator. Voltage comparators added to each phase compare the system voltage to the band limits, which helps determine whether a tap raise or lower operation must be carried out to bring the voltage in band. The intertap duration is a user-settable value. The tap raise or lower operations are contingent on which test scenario is being run, which is described in Section 10.3. The hardware functions "BLOCK" and "INHIBIT" have not been modeled because these functions are not significant to the tests being performed in this section.

10.2.3 Voltage Controller

The voltage controller block on RSCAD continuously monitors the voltage at the reference point of the circuit and switches the DER and voltage regulator on or off to maintain the voltage within the specified band setting. An out-of-band condition would trigger the DER to switch on first. A continued out-of-band condition would next trigger the voltage regulator. The DER in the Volt/VAR mode and the voltage regulator tap changes would ensure that the voltage stays within the specified center band. The device that assumes primary control of voltage correction depends on the scenario, which will be discussed later in this section.

Figure 10.4 illustrates the voltage band check of the voltage controller block. The voltage location dial allows selection of a particular point on the circuit as the reference point for voltage regulation. In this study, the voltage at the end of the line was chosen as the reference voltage. The reference voltage is verified for an in-band or out-band condition. The pickup and dropoff timer at the end of the voltage band check ensures that the voltage is in that band for a certain time interval before asserting. This is especially critical if the DER comes online and takes a few cycles to stabilize to the desired reactive power output.

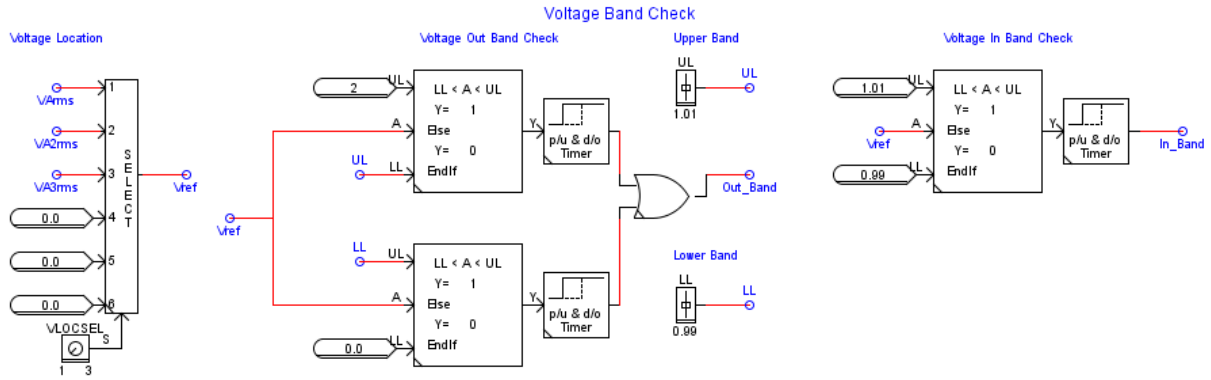


Figure 10.4: Voltage Band Check

Figure 10.5 illustrates the controller On/Off logic. The DER switches on only when the voltage has remained out of band for a certain amount of time. The voltage regulator switches on based on the scenario being run. Both the DER and the voltage regulator would switch off when the voltage comes back in band.

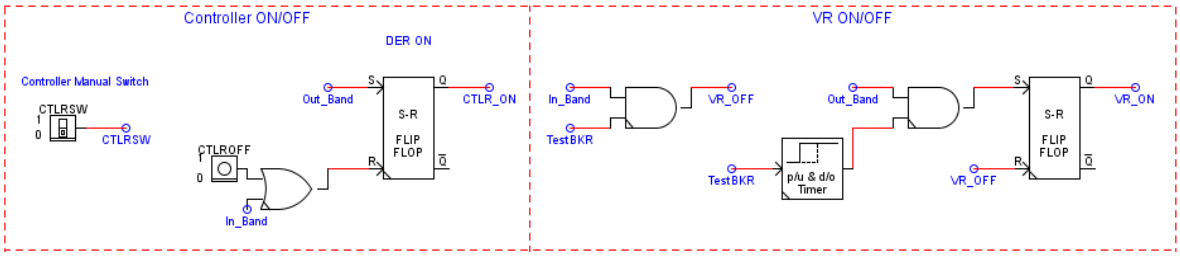


Figure 10.5: Controller On/Off Logic

Figure 10.6 illustrates the control logic for the voltage control Scenario 1. Scenario 1 involves the voltage regulator switching on after the DER has constantly been providing VARs for a prolonged period to help support system voltage. The DER, in this case, need not have achieved its maximum VAR capacity. This is particularly useful for cases in which the DER needs to be relieved from long-term voltage correction or to reduce the costs involved because of extended DER usage. In this scenario, the logic runs a check on the DER reactive power output for a specific period and triggers the voltage regulator to start raising or lowering its taps to bring the DER to an approximate zero VAR output, while at the same time ensuring that the system voltage stays in band. With each tap operation, more DER reactive power becomes available for future use. The DER remains the primary device for voltage correction for further voltage disturbances.

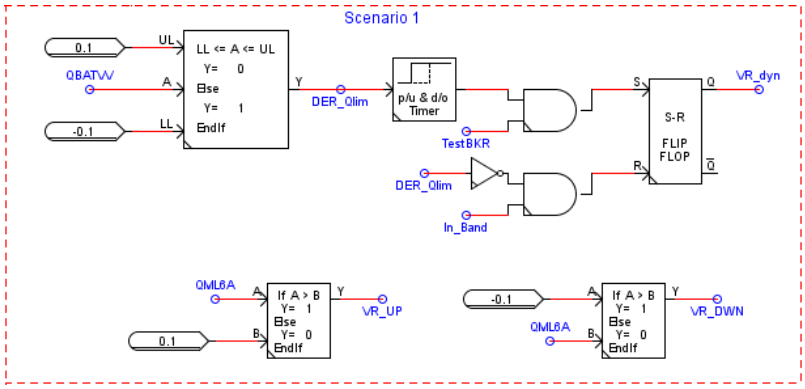


Figure 10.6: Voltage Control – Scenario 1

Scenario 2, shown in Figure 10.7, involves voltage regulator operation only if the DER is not able to support the system voltage. The system voltage going out of band would result in the DER switching on after a user-defined time interval. The DER would adjust its reactive power output to bring the system voltage in band. However, in a situation in which the DER attains it maximum VAR capability, the Scenario 2 logic would trigger the voltage regulator to come online and start raising or lowering its taps to reduce the DER output to zero, and at the same time bring system voltage in band. The voltage regulator is now the primary voltage corrector for any further voltage disturbances. The DER would only come back online when the voltage regulator has reached its maximum tap position. The DER allows for a faster and smoother voltage correction. The scenario selector selects the scenario to operate based on its input dial position.

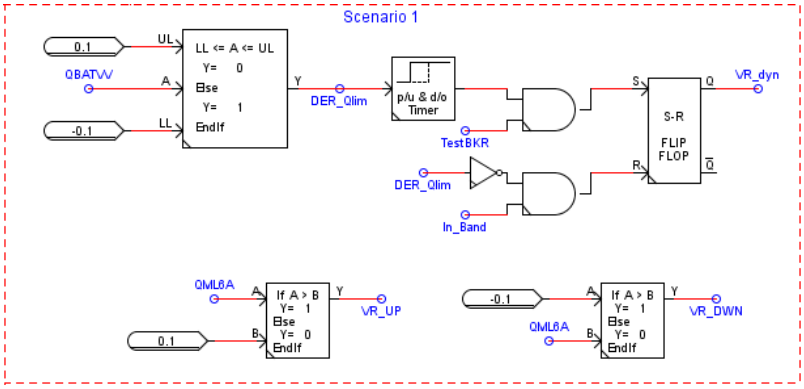


Figure 10.7: Voltage Control – Scenario 2

10.2.4 RSCAD RunTime

The RunTime screen for these tests is shown in Figure 10.8. It consists of controls for the circuit breakers and their status indicators. The controls described in Section 10.2.3 form part of the master controller. The load control has a selector switch to turn On/Off the 24-hour load profile and sliders to set the active and reactive power for the connected loads in the circuit. The inverter control sets the active and reactive power set point of the DER and includes a selector switch to toggle the Volt/VAR mode On/Off. Timers implemented in the DER logic can be controlled in the RunTime module.

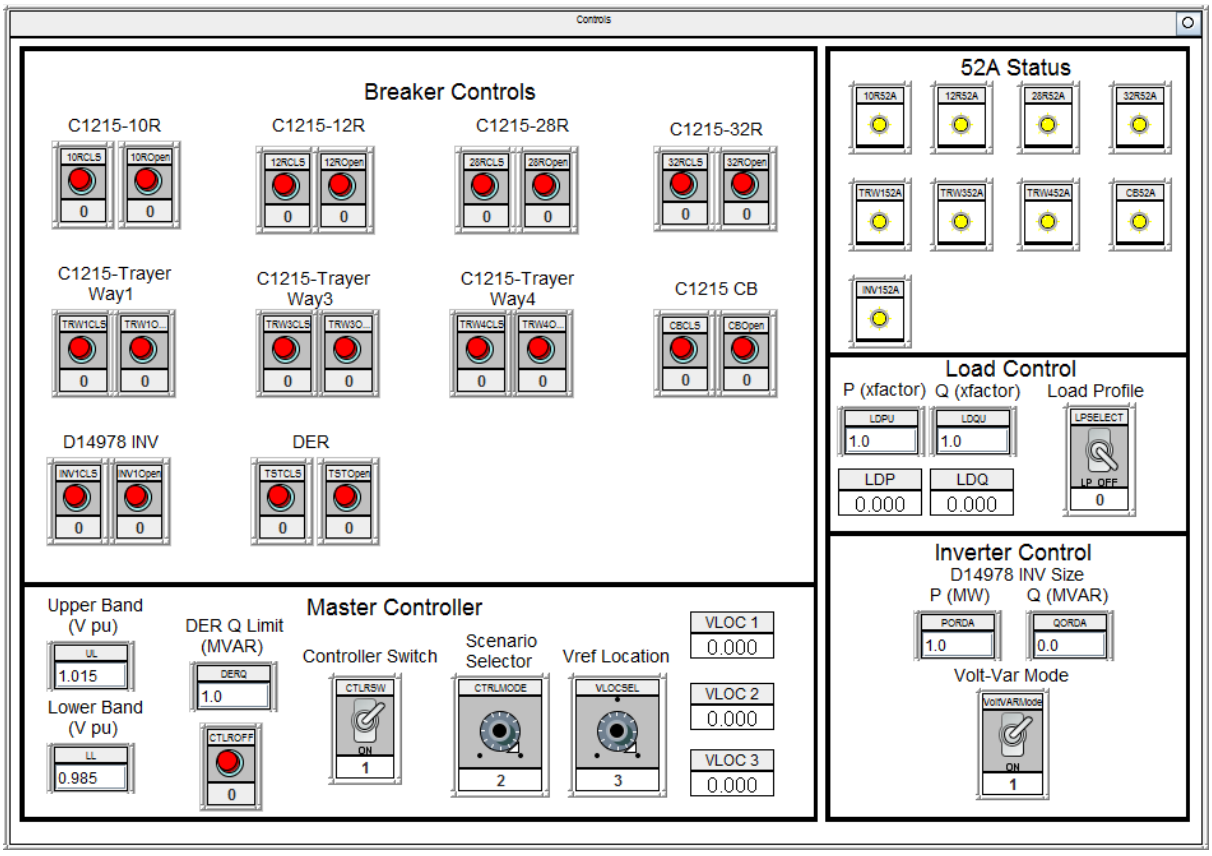


Figure 10.8: DER Test RunTime Controls

10.2.5 Hardware Implementation

The DER tests were performed on the RTDS using software models of the master controller, DER, and voltage regulator. The following are examples of devices that could be used for an actual hardware implementation of these tests. Appendix E – Proprietary Information includes a look-up table for the following devices:

- Master Controller – Device L1
- Voltage Regulator Control – Device L2
- Data Concentrator – Device L3
- DER – Device M

10.3 TEST PROCEDURE

The DER is running in parallel with the grid for these tests. The DER is set in the Volt/VAR control mode. Voltage disturbances are created in the system by switching loads in and out to vary the system voltage magnitude. Logic for controlling and coordinating the DER and the voltage regulator will be designed in RSCAD.

10.3.1 Load Switching

For this test, switch in a significant load that decreases the voltage magnitude below the set reference. Then, switch out the load in steps to bring the voltage magnitude above the set reference (see Table 10.1).

Table 10.1: Load Switching

<table>
<tr><td colspan="3">Objective: Verify that the DER and voltage regulator work together to support voltage during a step increase and decrease in load.</td></tr>
<tr><th>Test Initial Conditions</th><th>Test Actions</th><th>Observations and Results</th></tr>
<tr><td rowspan="2">1. System with nominal voltage condition.
2. Volt/VAR control mode enabled.</td><td>1. Switch in load in steps.</td><td>Scenario 1: VAR requirement is less than the VAR capacity of the DER.
1. Decrease in voltage magnitude.
2. DER increases reactive power to restore the voltage within band.
3. Although voltage already restored, the voltage regulator is triggered to respond after a user-settable delay to relieve the DER from long-term correction.
4. The voltage regulator continues to operate until the VAR output in the DER is reduced to a minimum.
5. For a further decrease in voltage, the DER acts as the primary voltage correction device.
Scenario 2: The VAR requirement is more than the VAR capacity of the DER.
1. Decrease in voltage magnitude.
2. The DER increases reactive power to maintain the voltage.
3. Study the interaction between the DER and voltage regulator. Coordinate and control these devices to support the system voltage:
a) The DER supports the system voltage until it attains the maximum rated VAR capacity.
b) A further decrease in system voltage results in the voltage regulator raising its taps after a user-settable delay, to support the voltage.
c) The voltage regulator would continue raising taps until the DER reactive power output reduces to a minimum.
d) For a further voltage decrease, the voltage regulator acts as the primary voltage correction device.</td></tr>
<tr><td>2. Switch out load in steps.</td><td>1. Increase in voltage magnitude when the loads are switched out.
2. Observe the DER and voltage regulator response for Scenario 1 and Scenario 2.</td></tr>
</table>

Figure 10.9 illustrates the timeline for the operation of scenarios 1 and 2. The side-by-side representation of these scenarios shows the difference in operation of the DER and VR based on the respective scenario.

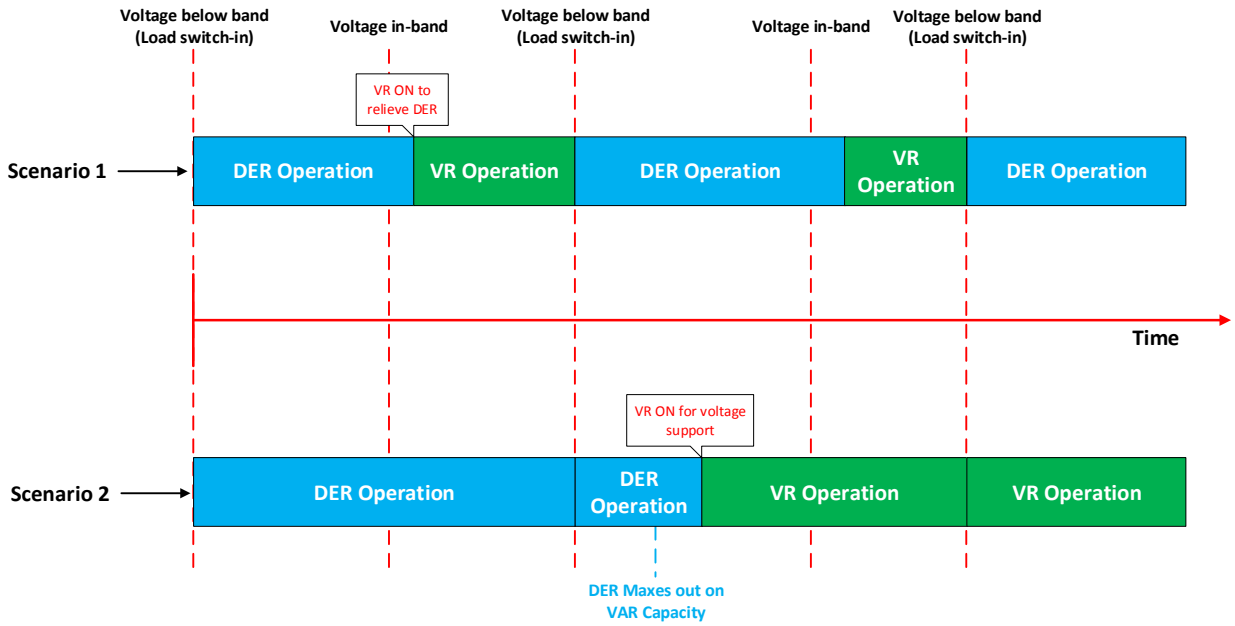


Figure 10.9: Voltage Support Coordination Scenario Operation

10.4 TEST RESULTS

10.4.1 Scenario 1

Scenario 1 was tested with the following assumptions. The system voltage is on a 12 kV base. The following set points are user defined and can be changed to values to best reflect field conditions.

Voltage upper band – 1.015 pu

Voltage lower band – 0.985 pu

DER MVAR limit – 1.0 MVAR

Voltage regulator on time delay – 10 seconds

Intertap delay – 4 seconds

Tests were carried out to validate the Scenario 1 operation with loads switched in and out in steps. To illustrate this scenario, the whole test has been broken down into eight individual events as illustrated in Figure 10.10. The following describes the circuit response and device operation during each event.

Initial Response

1. The test circuit is initially run at half the connected load capacity. The system voltage drops to below the In Band voltage setting. The DER switches on and increases the reactive power output to 0.65 MVAR to help bring the system voltage in band. The voltage controller sets the voltage regulator on standby.

2. The voltage regulator switches on after a user-defined time interval. The voltage regulator raises one tap to bring the reactive power output of the DER to zero and the system voltage in band. This ensures that the DER reactive power is made available for further voltage corrections. At the end of this event, the voltage regulator tap position is now one and the DER reactive power output is approximately zero.

Load Switch In Test

3. A large load is switched in, causing the system voltage to dip below the voltage lower limit. The DER increases its reactive power at once to help mitigate this event. The DER reactive power output attains its maximum capacity. At the end of this event, the system voltage is at 0.97 pu and DER output is at 1 MVAR.

4. Similar to Event 2, the voltage regulator starts raising taps to bring down the DER output and support the system voltage at the same time. The intertap time interval ensures that the DER and system voltage stabilizes before the next incremental tap operation.

5. At Tap 5, the DER output reduces to zero and the system voltage stays at approximately 0.998 pu.

Load Switch Out Test

6. A load-shedding event results in the system voltage rising beyond the upper limit of the In Band region. As a result, the DER reduces its reactive power output and starts absorbing reactive power to bring the voltage in band. By the end of the event, it was observed that the system voltage was at 1.01 pu with the DER at –0.84 MVAR. The voltage regulator is on standby for operation.

7. After the user-defined time interval, the voltage regulator starts reducing taps in steps to bring the DER reactive power output back to zero, while at the same time ensuring that the system voltage is brought back in band.

8. The voltage regulator has completed its tap operations, settling at Tap Position 3. The DER output is approximately zero and the system voltage is at 1 pu.

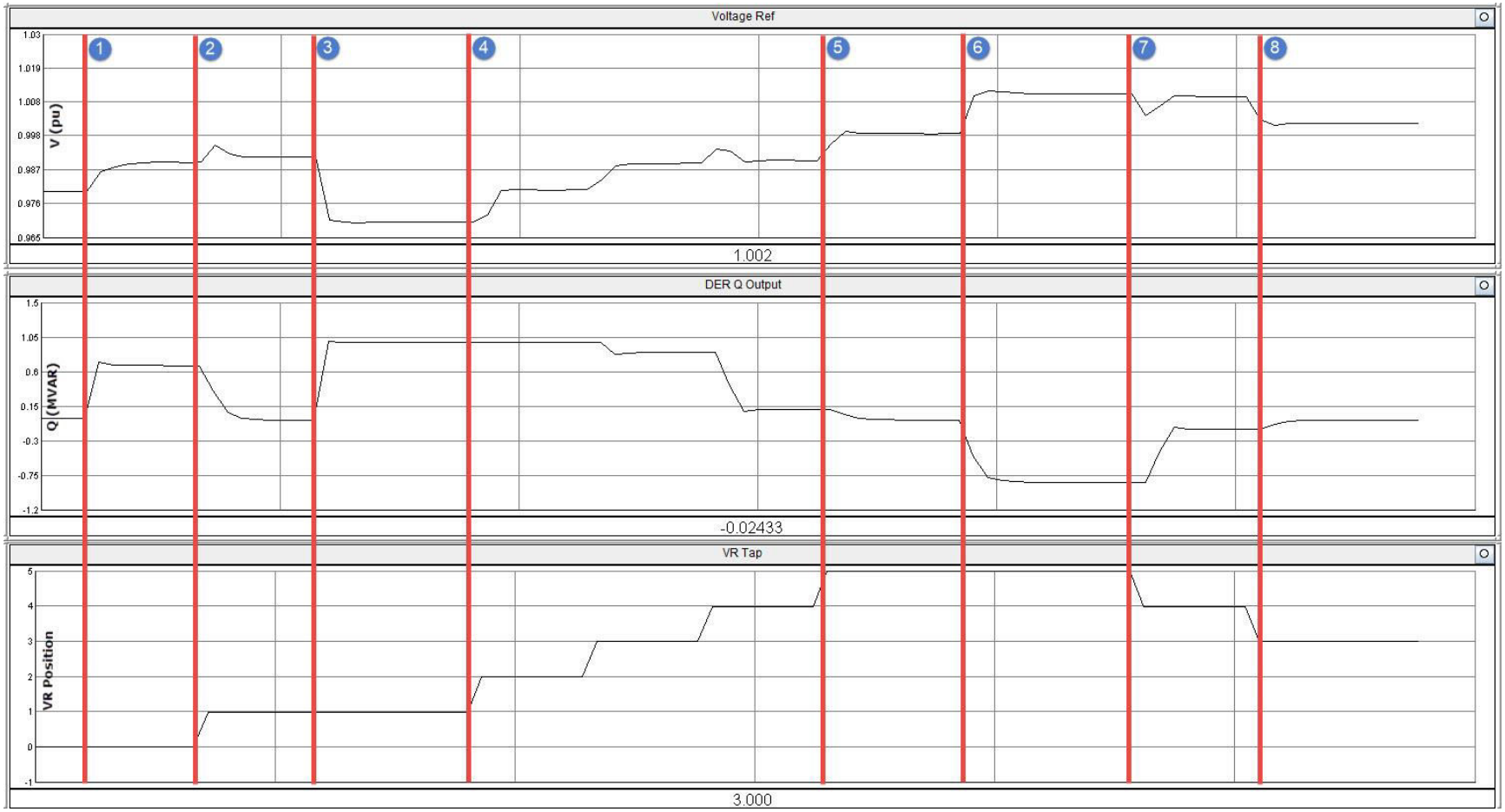


Figure 10.10: Scenario 1 RunTime Plot

10.4.2 Scenario 2

Scenario 2 was tested with the following assumptions. The system voltage is on a 12 kV base. The following set points are user defined and can be changed to values to best reflect field conditions.

Voltage upper band – 1.010 pu

Voltage lower band – 0.985 pu

DER MVAR Limit – 1.0 MVAR

Voltage regulator on time delay – 6 seconds

Intertap delay – 2 seconds

Tests were carried out to validate the Scenario 1 operation, with loads switched in and out in steps. Similar to Scenario 1, Figure 10.11 illustrates Scenario 2 with seven individual events. The following describes the circuit response and device operation during each event.

Initial Response

1. The circuit is initially run with half the connected load capacity. The DER is off, with the loads being fully supported by the utility. The system voltage falls below the lower voltage limit. The DER switches on after the specified DER switch on time, and increases its reactive power output to support the voltage to bring it in band. It was noted that the DER was able to support the system voltage before attaining its maximum VAR capacity. This event also illustrated that the volt/VAR control operates seamlessly to bring the DER reactive power output to a level that is just enough to support the system voltage. The voltage regulator remains off because the DER has not attained its maximum VAR capacity. At the end of this event, the DER reactive power output is approximately 0.66 MVAR and the system voltage is at 0.99 pu.

2. In this event, a large load is switched in to a point at which the DER would reach its maximum VAR capacity. The system voltage initially drops below the voltage lower limit, but picks up once the DER raises its reactive power output. The system voltage settles at 0.986 pu at the end of this event. The voltage regulator has not been triggered to operate.

Load Switch In Test

3. A further step increase in load results in the system voltage dropping out of band. The DER is already at its maximum VAR capacity. The voltage controller now begins to perform voltage checks to bring the voltage regulator online. The voltage regulator is now on standby to operate.

4. The voltage regulator, after a specific time interval, starts to raise its taps in steps, with each tap raise bringing the DER reactive power output down. This would continue until the DER reactive power output is close to zero and the voltage is brought in band. At the end of this test, the voltage regulator taps up to the fourth tap position, which results in a drop in the DER reactive power to zero VARs, bringing the system voltage to approximately 0.995 pu.

5. The DER has almost no reactive power output at this stage. The voltage regulator raise operation has ceased and stays at Tap Position 4.

Load Switch Out Test

6. This event illustrates the system response when loads are switched out. A step reduction in load results in the system voltage rising beyond the upper band limit, which in turn triggers the voltage regulator to lower one tap; thus, bringing the voltage in band. The DER does not operate because the voltage regulator has now assumed primary control for voltage correction. At the end of this event, the voltage regulator is at Tap Position 3 and the system voltage is at 0.99 pu.

7. Another step reduction in load results in a similar response as observed in Event 6. This illustrates that the voltage regulator is the first device to respond to a system voltage disturbance.

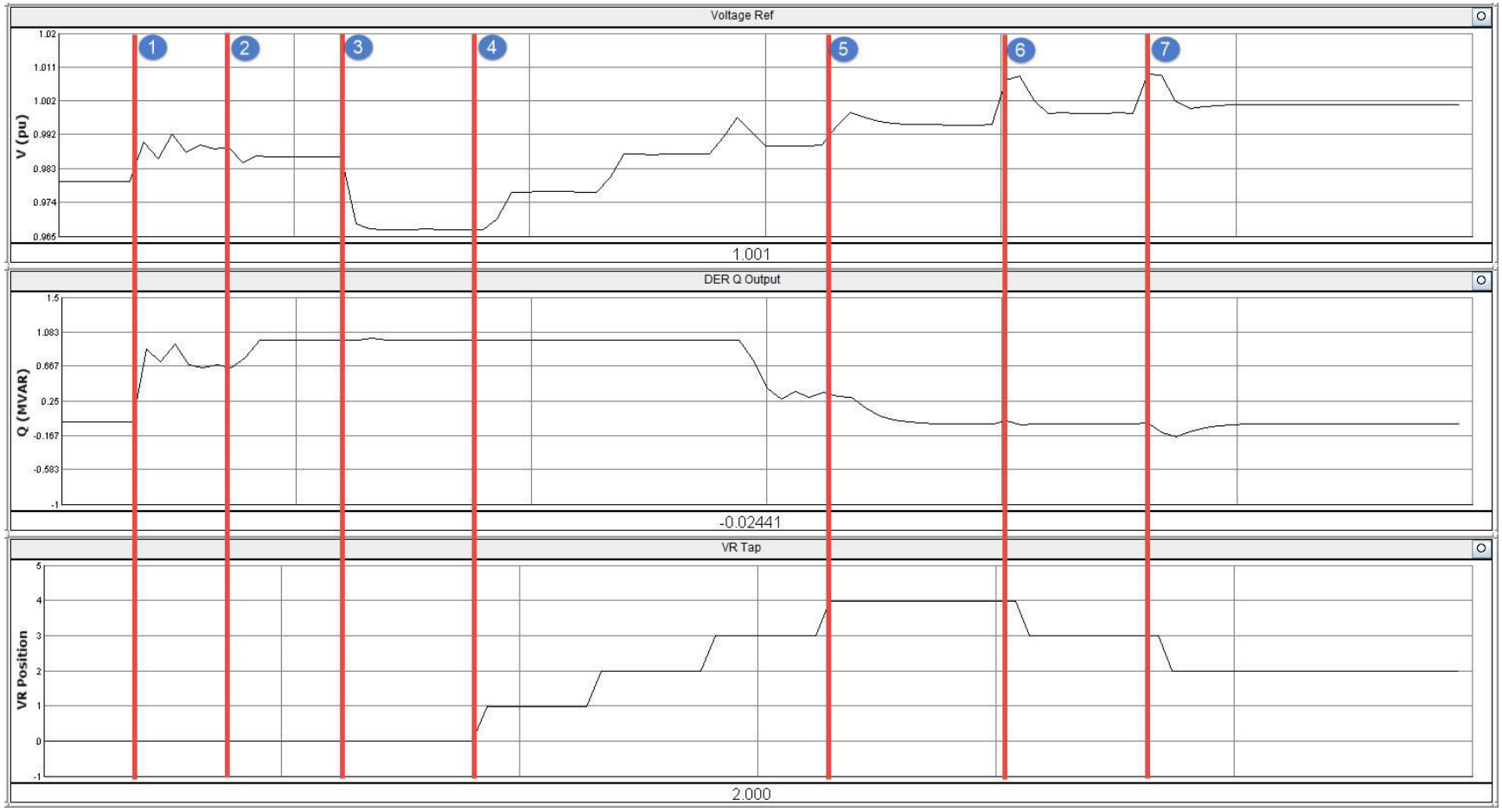


Figure 10.11: Scenario 2 RunTime Plot

11 FINDINGS

11.1 VOLTAGE COORDINATION TEST RESULTS ANALYSIS

The voltage coordination tests were carried out with two voltage correction devices, a DER and a voltage regulator, to demonstrate the implementation of a master controller to regulate system voltage in a distribution circuit. The master controller continuously monitors the voltage in the system and selectively switches the DER and voltage regulator to help mitigate a rise or drop in voltage. A tight voltage bandwidth was chosen for these tests to illustrate a successful operation of the voltage control. The controller operated seamlessly for various scenarios, providing useful information on the behavior of voltage correction devices and the coordination between them.

A DER and a voltage regulator on the selected desert-rural test circuit were found to be sufficient for voltage control. However, larger circuits may require multiple voltage correction devices such as DER, voltage regulator, and capacitor banks. These devices would be coordinated by the master controller. The voltage coordination test demonstration on the RTDS provides a good starting point for the implementation of a complex controller system for future implementations. This is further discussed in Section 12.1.

The Volt/VAR mode of the DER was observed to provide a smooth voltage correction as compared to the step-voltage correction of the voltage regulator. This can be seen in the Scenario 1 and Scenario 2 RunTime plots shown in Section 10. The scenarios tested employ the DER as the initial primary voltage correction device. It is recommended to have the DER continue as the primary voltage control device with the voltage regulator or other step-voltage controller brought in when the DER is not able to support the voltage.

The voltage regulator provides a good response to the voltage drop in the circuit and operates reliably when triggered by the master controller. However, for the desert-rural test circuit, the voltage regulator was observed to create a localized rise in voltage at its load terminals. This could be attributed to the fact that it regulates voltage in steps, with the rise or drop in voltage more pronounced at its load terminals; however, it reduces the voltage with loads downstream.

The DER tests were performed with selectable time delays on the controller operation and for the intertap delays for the voltage regulator. The time delays used in these simulations were selected to demonstrate the response of the master controller and the voltage correction devices. The intertap delay was added based on the field voltage regulator operation. For voltage regulators in the field, an intentional time delay is always included to avoid tap changer operation when the voltage excursion outside of the bandwidth is of a short duration. An example of such a case is a large motor starting on the system. The voltage level may be pulled low; however, it will be expected to recover in approximately 15 seconds. To have made a raise tap change within this short period would not significantly help in the motor starting and would require consecutive tap lowering operations after the motor came up to speed. This would also accelerate the wear of the tap changer. Consequently, an intentional delay is set at the discretion of the system operator, based on factors such as system loads, voltage regulation bandwidth, and voltage regulator response time. The software model time delay was found to respond accurately and can be adjusted to reflect the field voltage regulator settings. The time delays under discussion may need to be fine-tuned based on the industrial references and field operational practices.

11.2 VOLTAGE REGULATOR LOCATION ANALYSIS

The individual VR tests detailed in Section 6 reveal that SDG&E complies to the voltage regulation of ±5 percent, which equates to a forward bandwidth of 12 V, across the coastal-residential, urban and desert-rural circuits. However, it is recommended to narrow the forward bandwidth to allow for a better regulation. This would ensure less fluctuations in the regulated voltage and steady control over the standard voltage limits.

Section 10 includes pre-commercial voltage coordination tests that were carried out on the DER and voltage regulator on the desert-rural test circuit. The voltage regulator connected in the circuit helps regulate the voltage and bring it in band. Table 11.1 illustrates the voltage drop at various points of the circuit, with and without the voltage correction devices connected. Bus P40935A is connected to a long line section, which contains a considerable voltage drop.

Table 11.1: Desert-Rural Test Circuit Voltage Levels

Bus Name	% Line Lengths	Connected Load		Voltage Levels (pu)		
		P (MW)	Q (MVAR)	No DER	With DER	With VR
D1494793	1.65	1211	398	0.985	1.000	0.987
D1494794	1.79	331	108	0.985	1.000	0.987
D1494791	1.38	1542	506	0.985	1.000	0.987
P190655	9.14	105	35	0.985	0.999	0.987
P227957B	0.39	1647	541	0.986	0.999	0.988
CW	0.00	2186	717	0.987	1.000	0.988
P227958A	0.35	539	176	0.986	0.999	0.988
P41033	0.62	539	176	0.986	0.999	0.988
P41032A	0.93	539	176	0.986	0.999	0.987
P41032B	0.93	539	176	0.986	0.999	1.007
P41031	1.38	539	176	0.986	0.999	1.007
P190371	4.14	514	168	0.985	0.998	1.006
P208956A	5.46	419	137	0.985	0.998	1.006
P40934	8.26	419	137	0.984	0.997	1.005
P40935A	74.08	249	81	0.976	0.990	0.998
P40940	87.91	249	81	0.975	0.988	0.996
P40942	90.30	195	64	0.975	0.988	0.996
P45513	100.00	195	64	0.974	0.987	0.995
P40947	100.00	124	39	0.974	0.987	0.995

To mitigate this effect, it is recommended to add an additional voltage regulator at the midpoint of the line, at Bus P40935A. This would smooth the voltage along the long section of line and provide a better voltage regulation for the whole circuit. Moving the existing voltage regulator is not a solution because it goes beyond the area of influence of the DER. This would cause a section of the line to drop below the In Band voltage because the DER rated at 1 MW, 1 MVAR would not be able to support it.

In the pre-commercial voltage support coordination tests described in Section 10, the master controller regulated the voltage regulator taps based on the voltage at the end of the circuit. The voltage regulator tap operation is controlled by the master controller and operates to bring the voltage at the end of the circuit to within the voltage bandwidth. Voltage regulator advanced settings, such as line drop compensation and voltage limit, have not been considered for these tests. Figure 11.1 illustrates the voltage profile with the existing voltage regulator in service. There is a localized voltage rise at the load terminals of the voltage regulator. For the connected load and line length in this circuit, the voltage does not go beyond the In Band voltage range. However, for future expansion, with more loads and lines added to the circuit, the existing voltage regulator would create a localized voltage rise that could affect the loads connected near its load terminals.

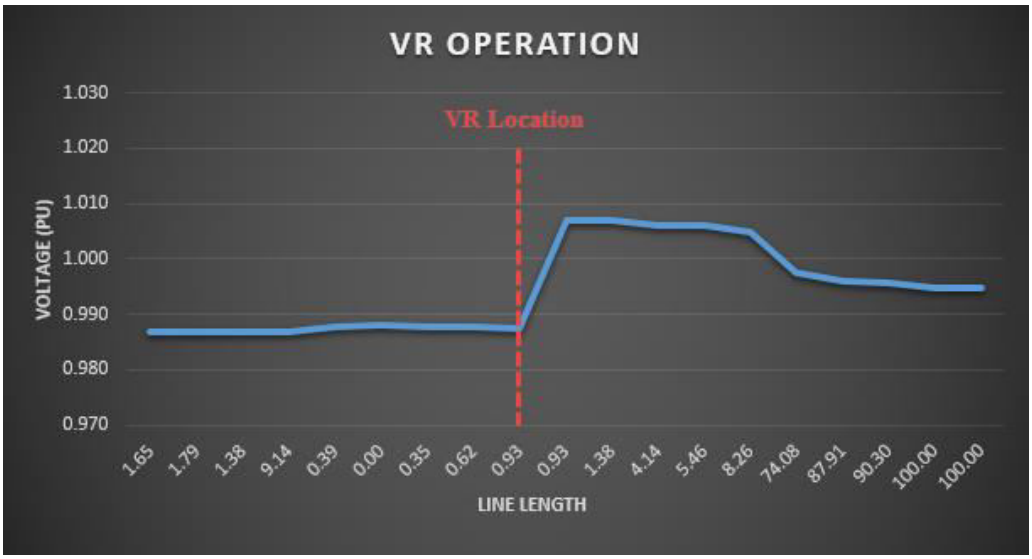


Figure 11.1: Voltage Profile With Voltage Regulator In Service

Refer to Appendix A for more information on the desert-rural test circuit one-line diagram.

For future implementation on larger circuits, it is recommended to connect multiple voltage regulators at various points of the circuit, based on the load and line impedance distribution in the circuit. The master controller would operate each voltage regulator based on the voltage drop at the next voltage regulator location, thus ensuring a much smoother profile. Voltage limit settings can be incorporated to ensure that the localized voltage drop or rise does not exceed stipulated limits.

12 RECOMMENDATIONS

The pre-commercial demonstration tests performed in this project lay the groundwork for commercial adoption of future smart circuit concepts. It is recommended that SDG&E pursue commercial adoption of some of the key concepts that were demonstrated. Specific recommendations follow in this section. Based on the findings and analysis of the demonstrations performed, recommendations on the integration and coordination of multiple voltage correction devices on a larger system, controlled by a central master controller, are described in this section. It was demonstrated via simulations that the DER and VR can be controlled interactively to provide voltage support on distribution circuits. Practical implementation and inclusion of other voltage correction devices are discussed. This section also describes certain modern solutions, such as downed conductor detection and power quality monitoring, which offers insights on how to improve existing distribution circuits.

12.1 SYSTEM VOLTAGE COORDINATION – ADVANCED CONTROL

Section 10 demonstrated the interaction and control of multiple voltage correction devices at a central level controller to maintain the system voltage within the specified band. The master controller discussed in Section 10 was designed with controls for coordinating a DER and voltage regulator for a voltage correction application. This was based on the desert-rural test circuit and provides a good insight into factors to examine for system voltage conditioning. Device factors such as real and reactive power capabilities, response time, device location, and smoothness of voltage correction play a big part in the addition to circuit parameters such as connected load and line impedances.

It is recommended to expand this concept to larger circuits that have multiple voltage correction devices such as multiple DERs, voltage regulators, and single-step or multistep capacitor controllers. Based on the results obtained from Section 10, it was observed that the DER was the first device to react to a voltage disturbance. Advanced controls can be implemented via a master controller at a central level that determine and control the switching priority of these devices based on the design philosophy. With this approach, the DER can be controlled to focus on the real power demand and devices such as voltage regulators and capacitor bank controllers can be controlled to focus on voltage correction. Other advantages of this scheme include monitoring and limiting frequent operation of any one device, which improves its lifespan and reduces frequent maintenance requirements. To achieve this scheme, it is important that these devices communicate at a central level.

Figure 12.1 illustrates the architecture envisioned to achieve the best practice recommended above. For this implementation, an automation controller capable of handling multiple communications protocols is considered as the master controller. Synchrophasor protocol based on IEEE C37.118.2-2011, IEEE Standard for Synchrophasor Data Transfer for Power Systems, is considered for data gathering from multiple field devices. IEC 61850 GOOSE protocol is considered for sending the switching controls from the master controller to the field devices.

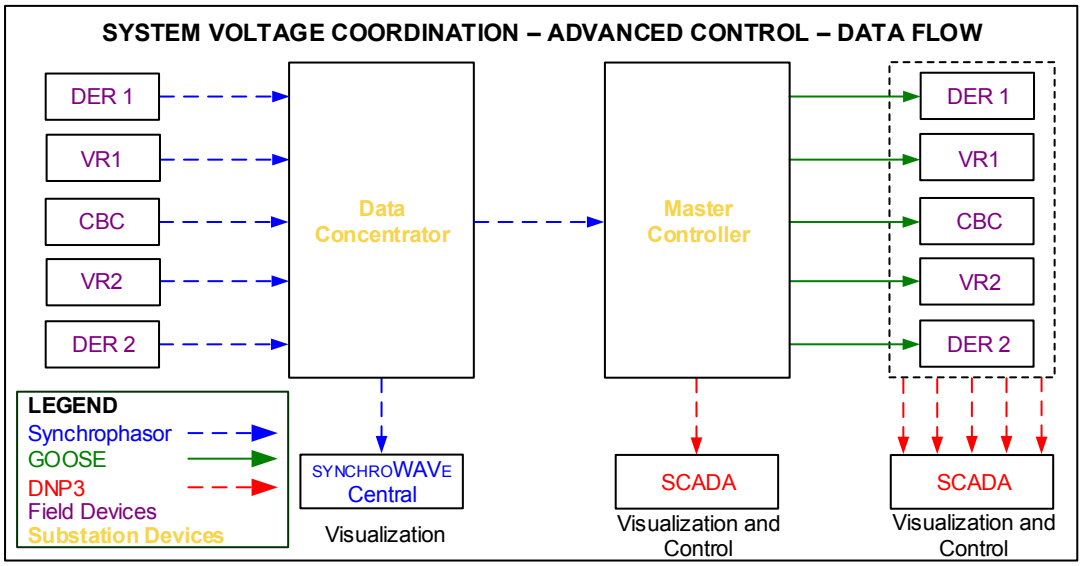


Figure 12.1: Data Flow for Advanced Control of System Voltage Coordination

Following is the description of the elements of the advanced control system illustrated in Figure 12.1:

- Field devices: DERs, voltage regulators, and capacitor bank controllers.
- Master controller: Automation controller.
- Communications protocol: Synchrophasor, IEC 61850 GOOSE, and DNP3.

The following path for data flow is recommended for this implementation:

- The field devices read currents and voltages via CTs and PTs that are wired to them.
- These data are collected and sent to the data concentrator located at a central location (possibly the substation) via synchrophasor protocol. This data stream carries the relevant phasor, analog, and digital information.
- The data concentrator collects the information and sends it over the to the master controller via synchrophasor protocol.
- The master controller uses this information in the algorithms that are specifically designed to determine the switching priority of these devices. The switching controls are sent back to the field devices via GOOSE protocol. This step closes the loop of data flow.
- For visualization, two paths are recommended:
  - Implementation of tools capable of providing instant access to real-time and historical data. This can be implemented for system-wide monitoring and analysis.
  - A traditional SCADA setup implemented via DNP3 protocol between the individual field devices and the SCADA, as well as the master controller and the SCADA.

The protocols and devices considered in this section are selected specifically for this discussion. This concept can be extended to other devices and protocols supported by various vendors. Based on the understanding and research carried out as a part of this project, it is recommended to implement the above discussed best practices to the already existing infrastructure at San Diego Gas & Electric. This is a cost-effective and efficient way to proceed with the commercial implementation of the recommended best practices.

Some of the challenges associated with implementing this concept to larger circuits include bringing together devices from multiple vendors on one platform and the communications protocols supported by them. As a step in commercial adoption, it is recommended to evaluate the selected devices and protocols, as well as the communications delays associated with the selected devices and protocols, before implementation. Refer to Section 13 for the technology transfer plan recommended for successful commercial implementation of the voltage support coordination scheme.

12.2 DOWNED CONDUCTOR DETECTION

From the pre-commercial tests performed on HIF detection, it is recommended that SDG&E monitor the coastal-residential, urban, and desert-rural test circuits carefully for HIFs. The tests showed that the high-impedance protection works as expected and can be used to indicate how the SDG&E circuits will behave in the event of an HIF. It is recommended to observe and fine-tune the HIF settings that are needed for each circuit.

With an extensive amount of overhead power lines across the country, the hazards of downed conductors cannot be overlooked. A weather-related or accidental incident can bring live conductors crashing to the ground. If still energized, these pose dangers to human and animal life and cause forest fire hazards, especially in dry regions (Figure 12.2). Utilities need to be able to quickly repair a broken line. To do so, they must be able to detect the downed conductor and its location at the earliest moment.

An HIF occurs in the event of an energized conductor making unwanted ground contact. Unfortunately, there are chances an energized broken conductor may go undetected with conventional overcurrent relays because the measured fault currents are very low. Several technologies have been developed to detect HIFs. In any scenario, the detection and isolation will take effect only after the live conductor has hit the ground and has created potential safety hazards, even if it is for a brief amount of time. Much time and effort has been dedicated by utilities and manufacturers toward developing methods for quickly detecting and isolating these faults.

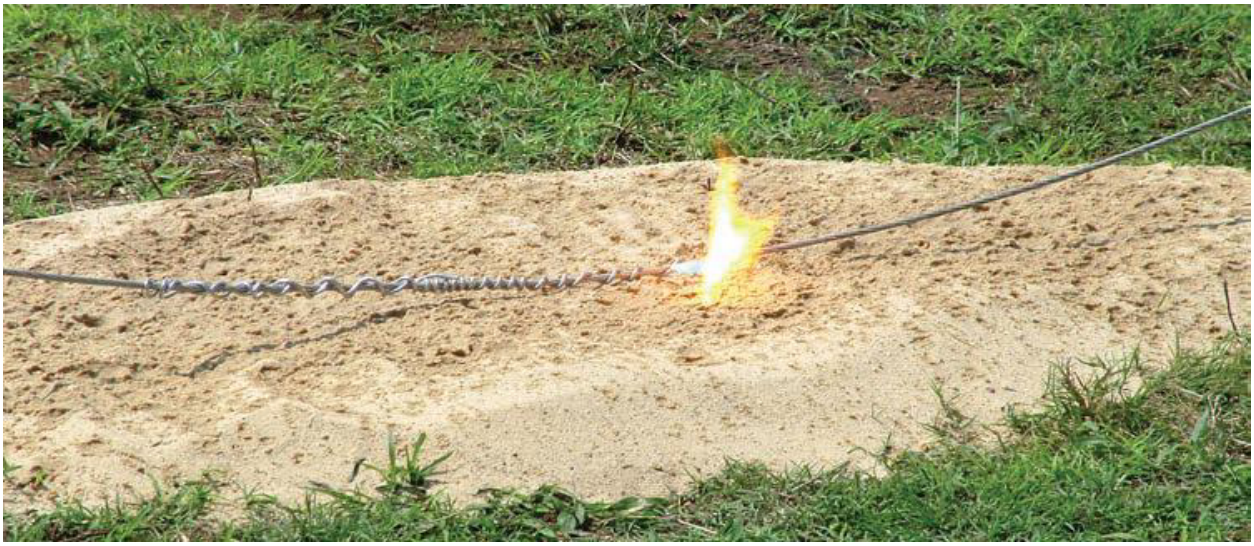


Figure 12.2: Energized Downed Conductor Causes Arcing – Potential Safety Hazard

With advancement in technology and availability of fast-speed communication, falling energized conductors can be detected and isolated before they hit the ground. Protection schemes have been developed that identify the break of a phase conductor and trip the affected section of the circuit in the small time window between the moment of the break and the time the conductor hits the ground. The result of this is that the conductor is de-energized when it hits the ground, thereby eliminating the risk of arcing or the presence of energized conductors on the ground.

The protection philosophy previously described makes use of IEDs with the ability to stream PMU data and central controllers with high-speed Ethernet radio communication. IEDs capable of synchrophasor communication and IEC 61850 GOOSE may already be present on several SDG&E distribution circuits, performing other protection and automation functionalities. The existing infrastructure can be enhanced to perform the falling energized conductor detection. Circuit IED PMUs may include substation protective relays on the breaker of the circuit, recloser controllers, capacitor bank controllers, voltage regulators, et cetera. The data from the field devices are collected by a data concentrator, which in turn transfers it to the central controller. Falling energized conductor detection algorithms are located within this central controller. Post detection, controls to isolate the affected section of the circuit are sent to the relevant field PMUs by the central controller. Synchrophasor protocol may be implemented to gain a deeper insight into the distribution system for visualization.

Figure 12.3 illustrates a conceptual distribution circuit with Source A and Source B. Once the broken conductor is detected by the central controller, PMU3 and PMU4 will trip and isolate the affected section. The loads on either side of the affected sections will continue to be supported by the two sources.

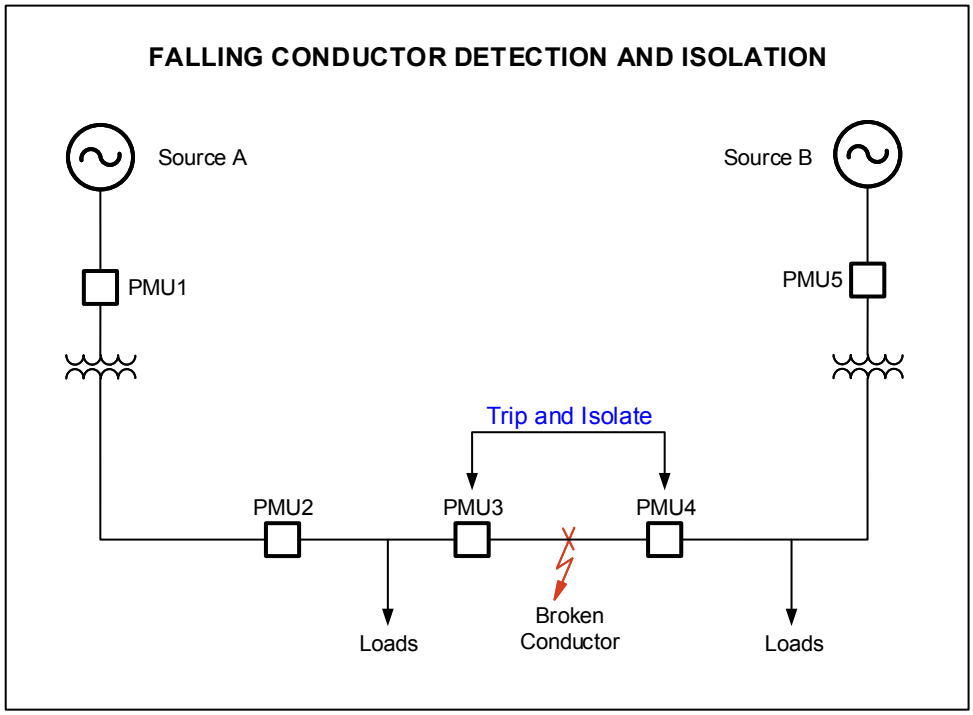


Figure 12.3: Falling Conductor Detection and Isolation

12.3 ISLAND DETECTION – VECTOR SHIFT ELEMENT

Certain feeder protection relays have the vector shift element feature that is used to detect islanding conditions of distributed generators (DGs) or loss of mains, and disconnect these DGs from the utility network under these conditions. The vector shift element is designed for applications where a DG is connected to either the utility of other main generators that require fast disconnection upon detection of an islanding condition. The element operates within 3 cycles, providing fast and reliable island detection; it operates fast enough to prevent out-of-synchronism reclosing of network feeders and thereby avoiding generator damage and any adverse effects. It is recommended that SDG&E explore commercial use of the vector shift element feature.

12.3.1 Vector Shift Element Logic

The vector shift element detection occurs when there are sudden phase variations on all three phases of the voltage waveforms. At the instance of islanding, the sudden change in load current causes a sudden change in the periods of the voltage signals. This element measures the difference in the present period duration and a reference period. This difference is then converted into degrees and compared against a user-defined setting.

Figure 12.4 describes the vector shift element logic. The element performs period calculations on each of the voltage inputs: VA, VB, and VC. The zero-crossing detector performs the period calculations. The time stamps of two consecutive positive or negative zero crossings are used to determine the period. The relay establishes a reference period for each phase using the previous 32-period measurement. The initialization period for this element requires at least 16 cycles of voltage signal to establish an accurate reference period. During the initialization period, this element does not detect an islanding condition.

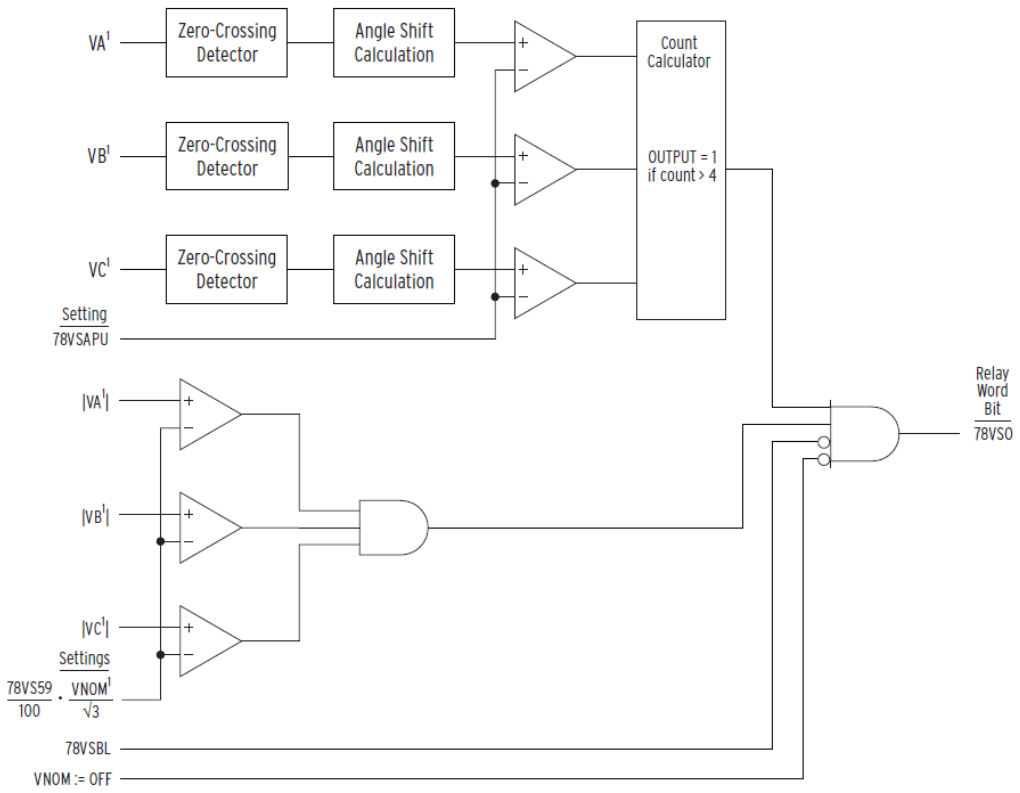


Figure 12.4: Vector Shift Element Logic

In each quarter cycle, the relay calculates the difference between the present period on each phase with the corresponding reference period. This difference is expressed in degrees to determine the angle shift and compared against the setting 78VSAPU. The count calculator increments each time the measured angle shift is greater than the threshold setting 78VSAPU. If the count exceeds four and no blocking conditions exist, the 78VSO asserts, indicating an islanding or loss-of-mains condition. The 78VS59 setting prevents false tripping under power system short-circuit conditions. The 79VSBL setting provides additional blocking conditions as required by the application used.

The vector shift element (78VS) and the fast rate-of-change-of-frequency element (81RF) can be used to detect islanding conditions. The vector shift element is designed to detect islanding at the instance of occurrence. It typically responds within 1.5 to 3 cycles after an islanding condition occurs. Conversely, the 81RF is designed to detect islanding conditions during and after the voltage shift occurs. The 81RF is used to compliment the 78VS element by providing more dependable protection.

12.4 ISLAND DETECTION – FAST RATE-OF-CHANGE-OF-FREQUENCY PROTECTION

Frequency changes occur in power systems when there is an unbalance between load and the active power generated, such as in an islanded condition. Typically, a generator control action adjusts the generated active power and restores the frequency to the nominal value. Failure of such a control action may lead to system instability unless remedial action is taken. The fast rate-of-change-of-frequency (df/dt) protection provides a fast response to islanding conditions, using the 81RF element.

Figure 12.5 shows the characteristic, based on frequency deviation from the nominal frequency (DF = FREQ – FNOM) and the rate-of-change-of-frequency (DF3C), to detect islanding conditions. The element uses a time window of 3 cycles to calculate the value of DF3C. Under steady-state conditions, the operating point is close to the origin. During islanding, the operating point typically enters Trip Region 1 or Trip Region 2 of the characteristic. The element uses the settings 81RFDFP in hertz and 81RFRP in hertz per second to configure the characteristic. It is recommended that SDG&E explore commercial use of the fast rate-of-change-of-frequency feature.

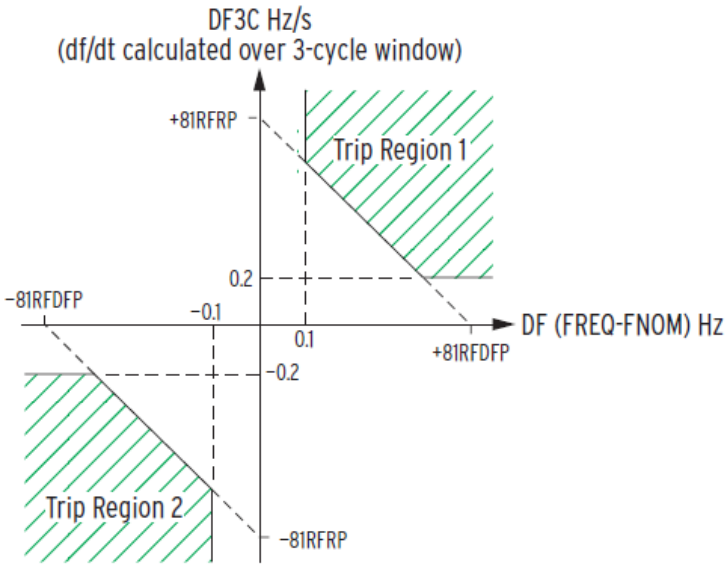


Figure 12.5: 81RF Characteristics

12.5 FAST DECOUPLING SCHEMES

Fast decoupling schemes are used to detect an island and to disconnect all loads, except the essential island loads, ensuring a stable power supply to these loads. A fast decoupling scheme makes use of the fast df/dt elements, along with synchrophasor quantities, to ensure a quick response during islanding. It is recommended that SDG&E explore commercial use of fast decoupling schemes feature.

12.5.1 Local Decoupling Protection Scheme

This decoupling scheme relies on local measurement only because the remote-end system information is not available. The following elements are enabled for this scheme:

- Df/dt
- Fast df/dt (81RF)
- Underfrequency (UF) and overfrequency (OF)
- Undervoltage (UV) and overvoltage (OV)

Figure 12.6 illustrates the decoupling curve for a case study. The under- and overfrequency elements are selected to coordinate with the generator protection at 59.5 Hz and 60.5 Hz, respectively, with a 12-cycle delay. Additional under- and overfrequency alarm elements are enabled with a 30-cycle (0.5 second) delay. In this decoupling scheme, df/dt is selected at 2.5 Hz/second with a 10-cycle delay and with a fast df/dt of 7.5 Hz/second with a –7.5 slope. This protection is found to be sensitive for weak system operating conditions, and operates accurately and faster than df/dt. This scheme adjusts the df/dt set point based on the deviation of frequency from the nominal frequency.

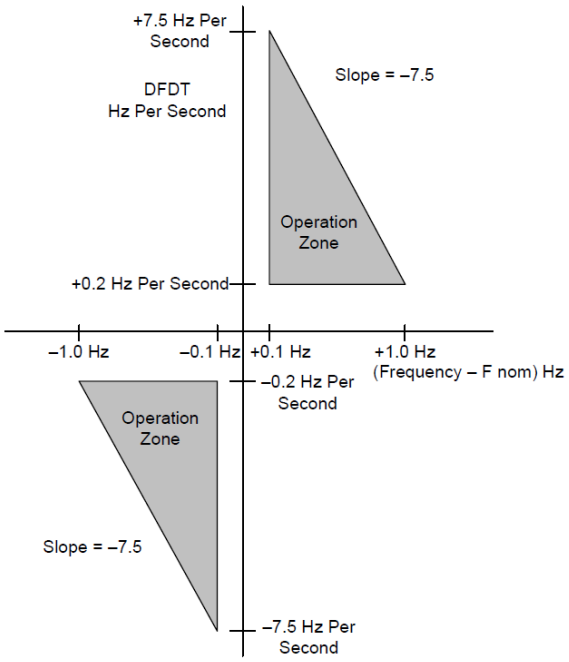


Figure 12.6: Fast df/dt Logic

12.5.2 Synchrophasor-Based Decoupling Protection

12.5.2.1 SYNCHROPHASOR PROTOCOL

The synchrophasor protocol makes use of synchronized phasor measurements, as well as the message format to communicate data in a real-time system. A synchrophasor stream consists of synchronized measurements of voltage phasors, current phasors, and frequency with the UTC as a reference for measurement. IEEE C37.118 and IEEE C37.118a, IEEE Standard for Synchrophasor Measurements for Power Systems – Amendment 1: Modifications of Selected Performance Requirements, define the synchrophasor protocol. Synchrophasors have applications in wide-area power system monitoring and analysis. Traditional information management systems such as DNP3, Modbus, and object linking and embedding (OLE) for Process Control (OPC) communicate information back to a central station, only in magnitude measurement. These systems update every few seconds to every few minutes. These data are not time-stamped, which makes it difficult to accurately determine the system conditions. Synchrophasor measurements help overcome these shortcomings. Synchrophasors can be placed at various points in the power system, collecting critical system data and sending the data to the central station, via synchrophasors, for dynamic system analysis.

12.5.2.2 SYNCHROPHASOR-BASED DECOUPLING PROTECTION

The local-based protection will not operate accurately for system conditions when the load flow on the tie lines between two systems is low and the remote-end breaker opens. During this condition, because the tie line is floating, the local operating quantities such as voltage, frequency, df/dt, and fast df/dt will not see adequate change to operate. In such an operating condition, the remote substation information and breaker statuses are required to correctly determine an islanding condition. When the remote-end breaker opens, the frequency between the substation slips; however, it is not fast enough to trigger the local decoupling protection. Having synchrophasor

communication between these two substations helps detect an islanding condition and to decouple the system faster and more reliably as compared to the local, fast decoupling scheme. Synchrophasors installed at the local end and remote end continuously collect synchrophasor data and send the data to a central controller. For the condition previously discussed, when the difference in frequency between the local end and remote end goes beyond a certain set point, the controller would be able to make a quick and accurate decision on decoupling the system.

12.6 POWER QUALITY MONITORING

There are several reasons to monitor power quality. The primary is the economics behind it, especially if critical process loads are adversely affected by poor power quality. The effect on equipment and process operation can include misoperations, damage, process disruption, et cetera. In addition, equipment damage and frequent repairs both cost money and increase down time.

Power quality monitoring is a very important aspect to be considered while providing reliable power to customers. In addition to resolving equipment disruptions, data monitored and collected over time can help in developing the equipment tolerances and sensitivity. This can provide a basis for developing equipment compatibility specifications for future equipment enhancements. It is recommended that SDG&E explore expanded power quality monitoring and additional uses of the power quality data.

Recording power system monitoring data over time is equally essential for analysis and resolving disruptions. Some of the power quality attributes that can be measured and recorded include the following.

12.6.1 Voltage Sag, Swell, and Interruption

According to IEEE 1159-2009, IEEE Recommended Practice for Monitoring Electric Power Quality, voltage sag is defined as a decrease in rms voltage to between 0.1 pu and 0.9 pu for durations from 0.5 cycles and 1 minute. Voltage sags are usually associated with system faults; however, they can also be caused by switching loads, starting significantly large motors, or can be related to weather disturbances, among other issues. Short-duration voltage sags are known to cause process disruptions in various industries.

Voltage swell is defined as an increase in rms voltage above 1.1 pu for durations from 0.5 cycle to 1 minute. Swells can be caused by switching off a large load, load shedding, or switching on a large capacitor bank. An increase in voltage applied to equipment above its nominal rating may cause failure of the components, depending upon the magnitude and frequency of occurrence.

Voltage interruptions are defined as a decrease in supply voltage to less than 10 percent of nominal for a period in excess of 1 minute. These may affect electronic and lighting equipment and cause misoperation or shutdown.

12.6.2 Harmonics

Harmonics are sinusoidal voltages or currents having frequencies that are integer multiples of the frequency at which the supply system is designed to operate. Power electronics-based equipment is a major contributor of harmonics in the power systems. Harmonics injection can cause overheating of rotating equipment, transformers, and premature failure of protective devices. IEEE 519-2014, outlines typical harmonic current limits for customers and voltage limits for supply voltage. Customers and electric power providers should attempt to operate within these limits to minimize the effects of harmonic distortion on the supply and customer end of the utility.

12.6.3 Unbalance

Voltage unbalance in three-phase systems is defined as the ratio of the magnitude of the negative-sequence component to the magnitude of the positive-sequence component, expressed as a percentage. Typically, the voltage unbalance of a three-phase service is less than 3 percent. Large single-phase loads can lead to higher unbalance in the system. High-voltage unbalance can lead to power supply ripple and heating effects on distribution equipment, which in effect may shorten equipment life.

Smart meters can be employed at key locations on a distribution circuit to monitor and record the previously mentioned parameters. It would be efficient to include tools that can retrieve power quality data captured by

individual meters located in the field, at a central level. This will assist in device management and monitoring on one convenient interface, instead of several individual sites. Automatic data collection improves efficiency by eliminating the time spent in the field manually collecting data from devices.

It is recommended that data collection tools be implemented to automatically collect power systems data. These data can be viewed and organized with the help of meter report software in the form of currents, voltages, harmonics, frequency, sag, swell, and interruption trends. Interactive charts and flexible report structures help manage data easily using a single interface (refer to Figure 12.7).

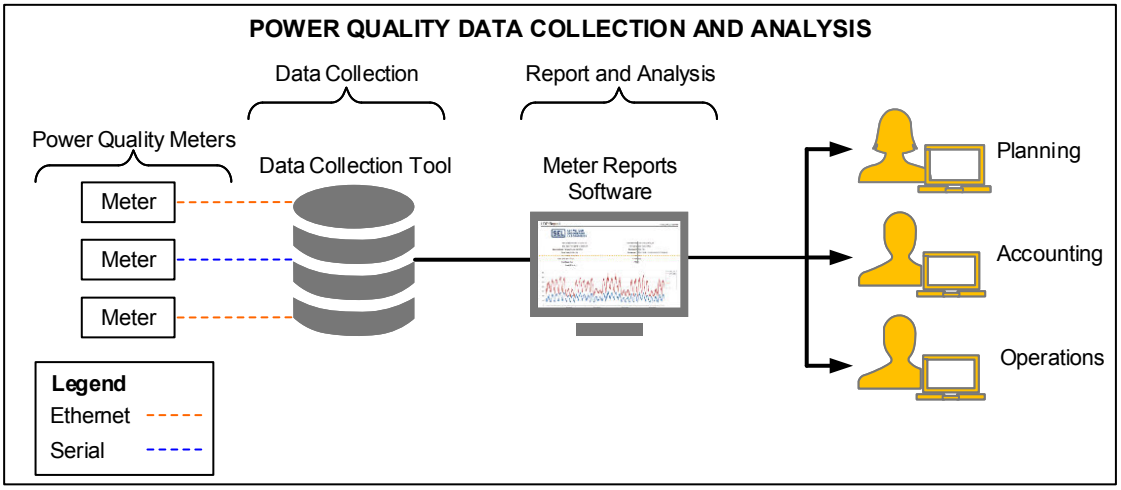


Figure 12.7: Power Quality Data Collection and Analysis

Refer to Section 9 for detailed results on power quality monitoring in the desert-rural test circuit. Circuit parameters such as voltage and frequency were observed at the time of switching in and out of an intentional island. System harmonics were not monitored because the RTDS model does not consider any source or load harmonics.

13 TECHNOLOGY TRANSFER PLAN

13.1 INTRODUCTION

The Technology Transfer Plan lists the steps for commercial adoption of the best practices discussed in this report. This plan describes the activities, equipment, and resources involved and the required coordination between diverse groups to successfully implement the best practices commercially.

13.2 PROCEDURE FOR COMMERCIAL IMPLEMENTATION

This report discusses the demonstration of the voltage support coordination scheme, including two voltage support devices and a central master controller, with the help of RTDS. The technology transfer plan bridges the gap between the laboratory demonstration of the voltage support coordination scheme and its successful commercial implementation in the field on larger distribution circuits with several voltage support devices. The design for the layout is described in the following subsections.

13.2.1 Design and Review

- *Distribution circuit selection*: This is the first step towards field implementation of the scheme. A distribution circuit will be selected based on the criteria that it includes a few voltage support devices. A simplified one-line diagram will be created to represent the voltage support devices, loads, sources, and any other information that may be relevant to the case.

  Device and communications protocols: This is a very important step because it is the design foundation of the scheme. Existing field voltage support devices will be evaluated for the features and functionalities that they offer. This will be a good time to perform any device upgrades, if required. The vendors and device recommendations for the master controller will be reviewed and finalized. The recommended communications protocols will be reviewed. Appendix E – Proprietary Information includes a list of recommended devices (Device L1, Device L2, Device L3, and Device M) for field implementation. Once the devices and communications protocols are finalized, a system architecture will be created defining the communications paths.

- *Enhancement of algorithms*: The algorithms developed in this project will be enhanced and the voltage support coordination philosophy will be reviewed to include multiple voltage support devices. This will mark the end of the design and review phase.

13.2.2 In-house Testing and Validation

- *RTDS model development and integrated testing*: The selected distribution circuit will be modeled in the RTDS. Once the algorithms are finalized, test equipment will be assembled for integrated RTDS testing. The voltage support coordination scheme will be tested in the laboratory environment. This step validates the scheme for larger distribution circuits including several voltage support devices.

- *Results, observations, and analysis*: Results and observations from the tests will be tabulated for further analysis and improvements.

13.2.3 Field Implementation and Monitoring

- *Development of test plan*: A detailed step-by-step test plan should be developed to test and commission the scheme on the live distribution circuit in future work.

- *Monitoring and training*: The field operations on live distribution circuits, as a result of the voltage support coordination scheme, should be closely monitored and verified to work as expected for a substantial period of time. Training material should be prepared and delivered to operators from the distribution planning and operations group to bring them up-to-speed with the field operations and SCADA indications.

- *Standardization*: This step includes standardizing the process of design and field implementation such that multiple distribution circuits can be enhanced efficiently with the voltage support coordination scheme.

13.3 CHALLENGES

One of the challenges associated with implementing this concept on larger distribution circuits with several voltage support devices includes bringing together devices from multiple vendors on a single platform. It is pertinent that these devices speak the same language; namely, that they have compatible communications capabilities.

Seamless coordination between different working groups within the organization or third-party vendors is essential.

13.4 RESOURCES

The implementation of the voltage support coordination scheme requires collaborated efforts between different working groups. The facility, system, and the groups within an organization and their tasks are defined below. Although each group has an assigned task, coordinated efforts and discussion between the working groups on a regular basis are essential.

- *Test facility* with advanced infrastructure to assemble the required test equipment for validation of the scheme for larger distribution circuits including several voltage support devices.
- *System protection group* to review the voltage support coordination philosophy and finalize the device selection.
- *Information technology or communications specialists* to review the communications protocols and network design.
- *Distribution planning and operations* to work in coordination with the system protection group to review the voltage support coordination philosophy and the switching order of the voltage support devices.
- *SCADA and relay technicians* to assist in installation, programing, and testing of the devices on the distribution circuits.

13.5 CONCLUSION

Based on the understanding and research carried out as a part of this project, there is a possibility of making the recommended enhancements to the existing infrastructure on San Diego Gas & Electric distribution circuits. This will be a cost-efficient way to implement the recommended best practices.

Once the voltage support coordination philosophy is defined for a couple of circuits and tested with the help of integrated RTDS testing, and the scheme is validated for larger distribution circuits with several voltage support devices, further RTDS testing for more circuits may not be required. At this point, the scheme will be standardized and minimum changes should be made from one circuit to another.

14 OVERALL PROJECT CONCLUSIONS

SDG&E's EPIC-1, Project 5, on Smart Distribution Circuit Demonstrations was successfully completed and documented in this report. Phase 1 of the project covered the evaluation and documentation of products and technologies currently available for improved distribution circuit design, system operation, and protection. Emerging distribution circuit solutions and operation practices were discussed for maintaining reliable, uninterrupted energy delivery to the customers. Phase 1 provided the required background for shortlisting the devices that were eventually used for demonstration of advanced circuit concepts through laboratory simulations.

Phase 2 of the project included selection and modeling of three diverse SDG&E distribution circuits viz., coastal-residential, urban, and desert-rural in RSCAD environment for demonstration of advanced circuit concepts. The first phase of demonstrations included testing capabilities and controls of a voltage regulator, and a capacitor bank controller as stand-alone voltage support devices in a distribution circuit. These tests provided useful data for the development of the more sophisticated voltage support coordination scheme with multiple devices. The results from the tests carried out on voltage regulator control also provide suggestions for improvements for optimal performance. The observations and results captured were analyzed and the findings from stand-alone device testing provided inputs on how to tweak the existing circuits for improved reliability and performance.

The second phase of the demonstrations included development of algorithms to enable controlled switching of multiple voltage support devices on a distribution circuit using a central controller on RTDS platform. The pre-commercial laboratory demonstrations successfully lay out the groundwork required for commercial implementation of the scheme. A technology transfer plan was created to bridge the gap between the laboratory demonstration of the voltage support coordination scheme and its successful commercial adoption in the field on larger distribution circuits with multiple voltage support devices. On larger distribution circuits with multiple voltage correction devices, system-wide voltage coordination would be required for efficient and reliable service to the customers. This implementation will also aid in improving the lifespan of various distribution equipment, as well as lower the associated maintenance costs.

Phase 3 of the project included findings and recommendations from the test demonstration in Phase 2. The recommended system architecture for commercial implementation of voltage support coordination scheme is provided.

In addition to this, certain other advanced distribution solutions are also recommended. With large distribution circuits arises the challenge of detecting, locating, and isolating HIFs caused because of downed or broken energized conductors. An energized conductor on the ground for a brief amount of time may pose as a huge safety hazard to human and animal life. Solutions for the efficient detection of broken conductors at synchrophasor speeds were discussed.

Solutions were discussed on efficient and reliable ways to detect islands in existing and future circuits. Fast decoupling schemes are particularly effective in ensuring that an island is detected in a few cycles and all loads except critical island loads are disconnected. This allows for continuous and stable power supply to these loads.

Power quality monitoring is a very important aspect to be considered while providing reliable power to customers. In addition to resolving equipment disruptions, data monitored and collected over time can help in developing the equipment tolerances and sensitivity. The various power quality attributes were discussed in detail and recommendations were provided on the implementation of a system for centralized power quality monitoring and analysis.

15 METRICS AND VALUE PROPOSITION

15.1 PROJECT METRICS

The project tracking metrics included the milestones in the project plan. Technical metrics were developed to guide the actual demonstration work. In general, the ultimate measure of success was having a benchmark future distribution circuit design concept that helps advance future distribution system development. The circuit design can assimilate a wide variety of existing and emerging device types and has a protection system that allows this assimilation to be done without compromising reliability or safety.

Also, project results were submitted as technical papers and presentations for consideration by major technical conferences and publications.

The following metrics were identified for this project:

- **Economic benefits:**
    a. Reduction in electrical losses in the transmission and distribution system.
- **Safety, Power Quality, and Reliability (Equipment, Electricity System):**
    a. Outage number, frequency and duration reductions.
    b. Public safety improvement and hazard exposure reduction.
    c. Utility worker safety improvement and hazard exposure reduction.
    d. Reduction in system harmonics.
- **Identification of barriers or issues resolved that prevented widespread deployment of technology or strategy:**
    a. Description of the issues, project(s), and the results or outcomes.
    b. Increased use of cost-effective digital information and control technology to improve reliability, security, and efficiency of the electric grid (PU Code § 8360).
    c. Deployment of cost-effective smart technologies, including real time, automated, interactive technologies that optimize the physical operation of appliances and consumer devices for metering, communications concerning grid operations and status, and distribution automation (PU Code § 8360).
    d. Integration of cost-effective smart appliances and consumer devices (PU Code § 8360).
- **Effectiveness of information dissemination:**
    a. Number of information sharing forums held.
    b. Stakeholders attendance at workshops.
    c. Technology transfer.
- **Adoption of EPIC technology, strategy, and research data/results by others**
    a. Description/documentation of projects that progress deployment, such as Commission approval of utility proposals for wide spread deployment or technologies included in adopted building standards
    b. Number of technologies eligible to participate in utility energy efficiency, demand response or distributed energy resource rebate programs
    c. EPIC project results referenced in regulatory proceedings and policy reports

15.2 VALUE PROPOSITION: PRIMARY AND SECONDARY GUIDING PRINCIPLES

The value proposition is to address how the project met the EPIC principals.

Table 15.1 summarizes the specific EPIC primary and secondary principles advanced by the Smart Distribution Circuit Demonstrations Project.

Table 15.1: EPIC Primary and Secondary Guiding Principles

Primary Principals			Secondary Principals				
Reliability	Lower Costs	Safety	Loading Order	Low-Emission Vehicles / Transportation	Safe, Reliable & Affordable Energy Sources	Economic Development	Efficient Use of Ratepayers Monies
✓	✓	✓					

The Smart Distribution Circuit Demonstrations Project covers the following primary EPIC principals:

- **Reliability:** The results of this project demonstrates several scenarios and options with the possibility to improve power reliability and performance with system monitoring. Also, the observations and results captured were analyzed and the findings from stand-alone device testing provided inputs on how to tweak the existing circuits for improved reliability and performance.

- **Lower Costs:** Based on the understanding and research carried out as a part of this project, there is a possibility of making the recommended enhancements to the existing infrastructure. The implementation of some of the recommendations would aid in improving the lifespan of various distribution equipment, which in turn lowers the associated maintenance costs.

- **Safety:** As part of the recommendations, the downed conductor detection using high impedance fault (HIF). With large distribution circuits arises the challenge of detecting, locating, and isolating HIFs caused because of downed or broken energized conductors. An energized conductor on the ground for a brief amount of time may pose as a huge safety hazard to human and animal life. Solutions for the efficient detection of broken conductors at synchrophasor speeds were discussed.

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APPENDIX A CIRCUIT ONE-LINE DIAGRAM

The following three simplified one-line drawings are drafted in Microsoft Visio software. Each diagram represents an SDG&E circuit that was modeled in RSCAD to recreate and simulate the distribution system. Faults, high-impedance faults, and islanding are simulated in RSCAD. The circuits are:

1. Coastal-residential circuit – Figure A.1
2. Urban test circuit – Figure A.2
3. Desert-rural test circuit – Figure A.3

Note: It is recommended to print the circuit one line diagrams on a large sheet for clarity.

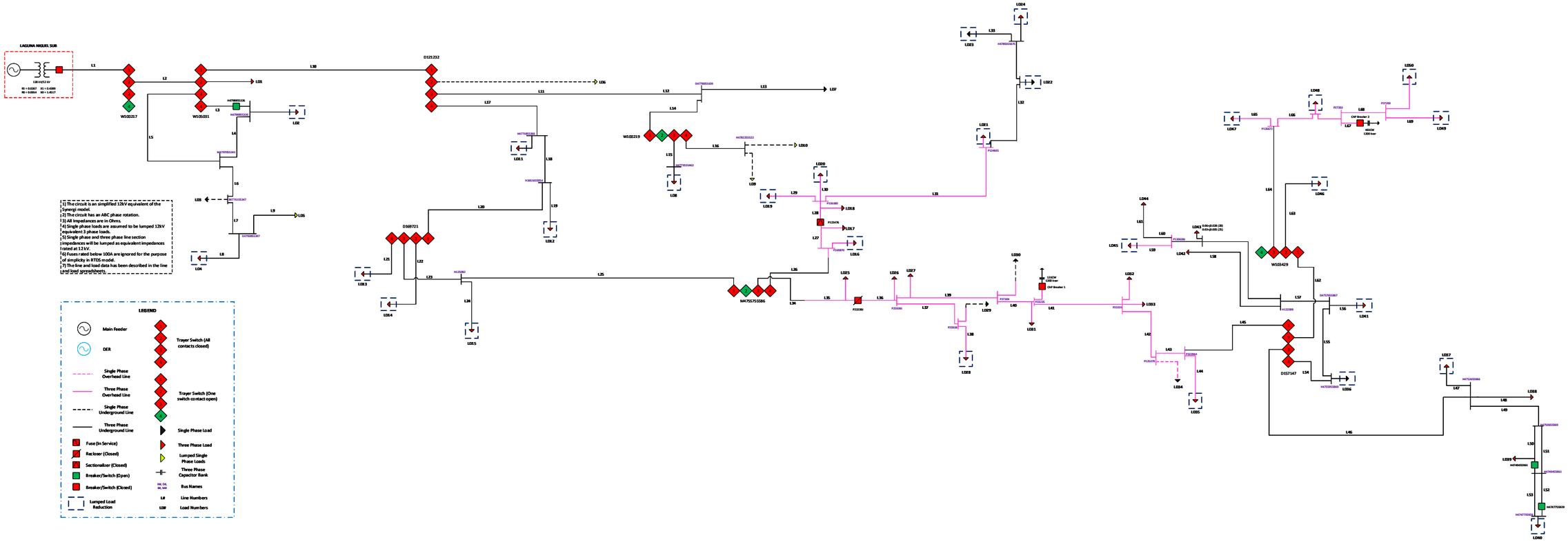

Figure A.1: Coastal-Residential Test Circuit One-Line Diagram

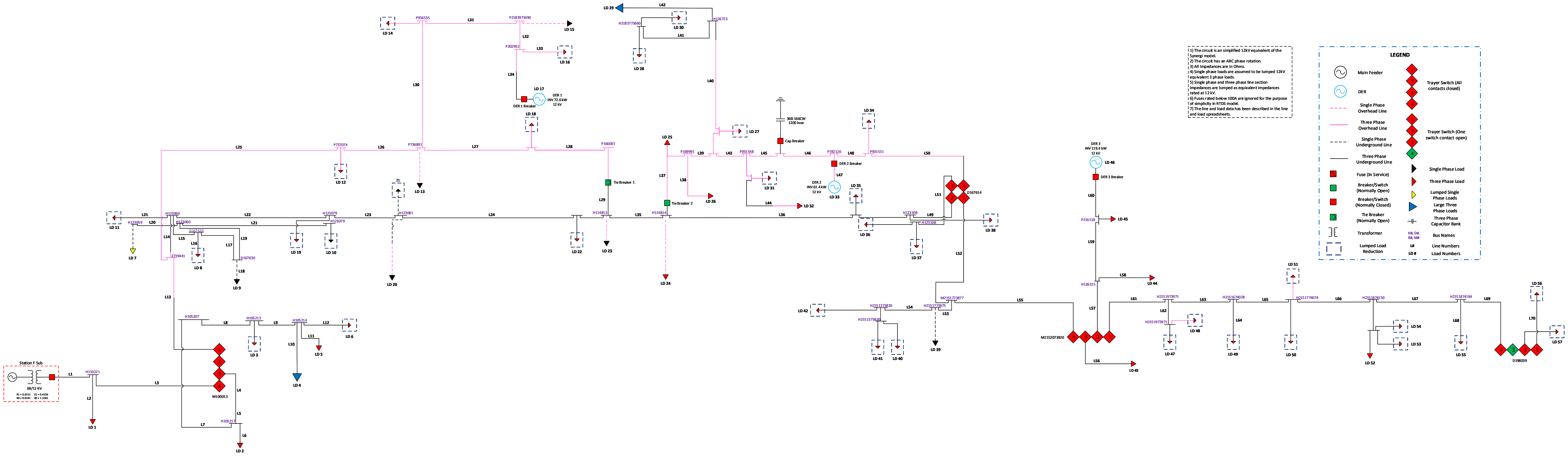

Figure A.2: Urban Test Circuit One-Line Diagram

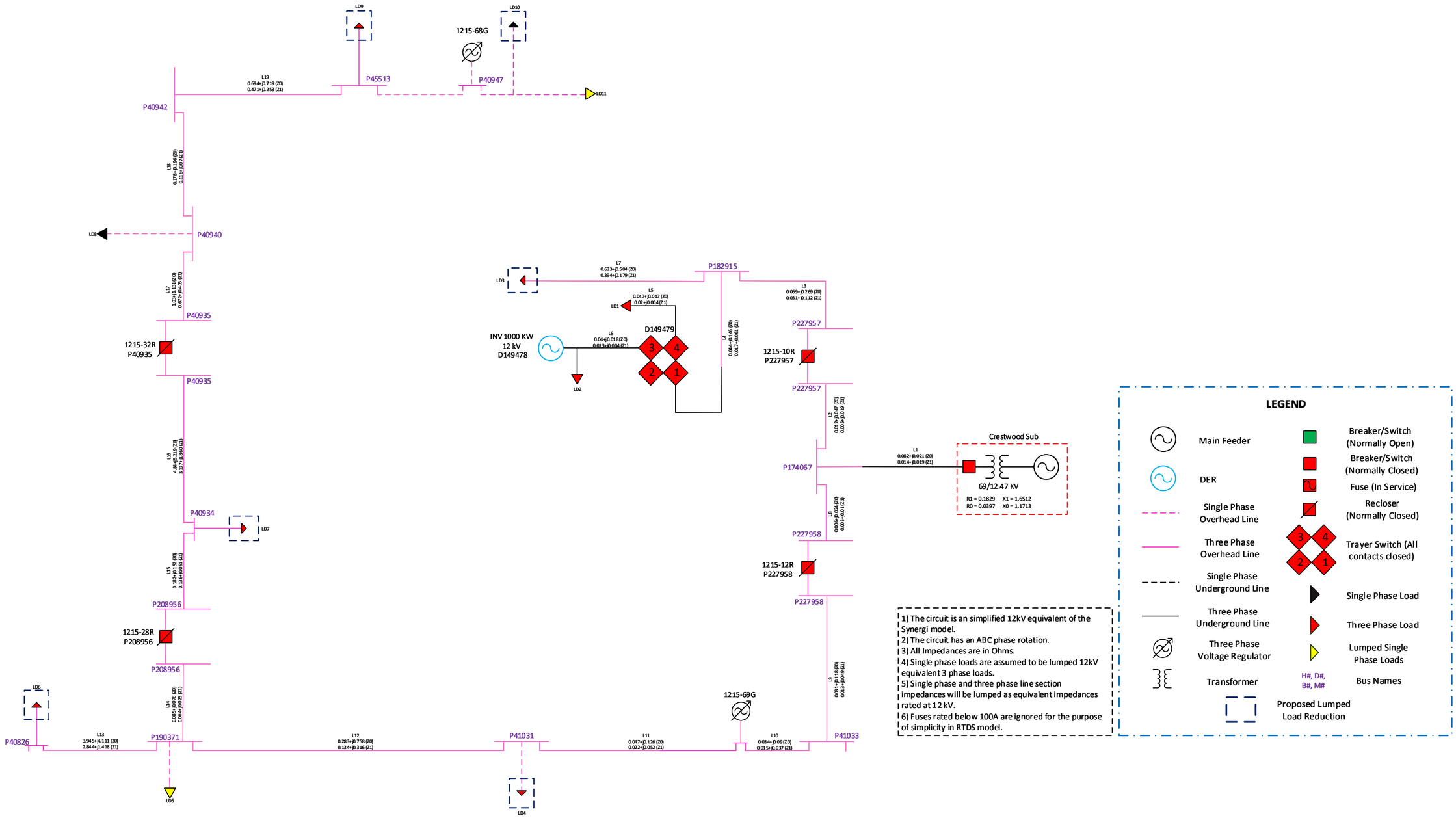

Figure A.3: Desert-Rural Test Circuit One-Line Diagram

APPENDIX B LOAD PROFILE

The following figures and tables show the actual load for a 24-hour period and the necessary slider position (in the digital simulator) required to obtain the condensed 60-minute equivalent load values. The tables are provided to show the specific slider settings necessary to get the desired real and reactive power setting output for RSCAD testing. The layout is as follows:

1. Coastal-Residential Test Circuit
    a. Figure B.1 – Actual Load Profile Over 24 Hours
    b. Figure B.2 – Actual Load
    c. Figure B.3 – Slider Position
    d. Table B.1 – Load and Slider Position Value
2. Urban Test Circuit
    a. Figure B.4 – Actual Load Profile Over 24 Hours
    b. Figure B.5 – Actual Load
    c. Figure B.6 – Slider Position
    d. Table B.2 – Load and Slider Position Value
3. Desert-Rural Test Circuit
    a. Figure B.7 – Actual Load Profile Over 24 Hours
    b. Figure B.8 – Actual Load
    c. Figure B.9 – Slider Position
    d. Table B.3 – Load and Slider Position Value

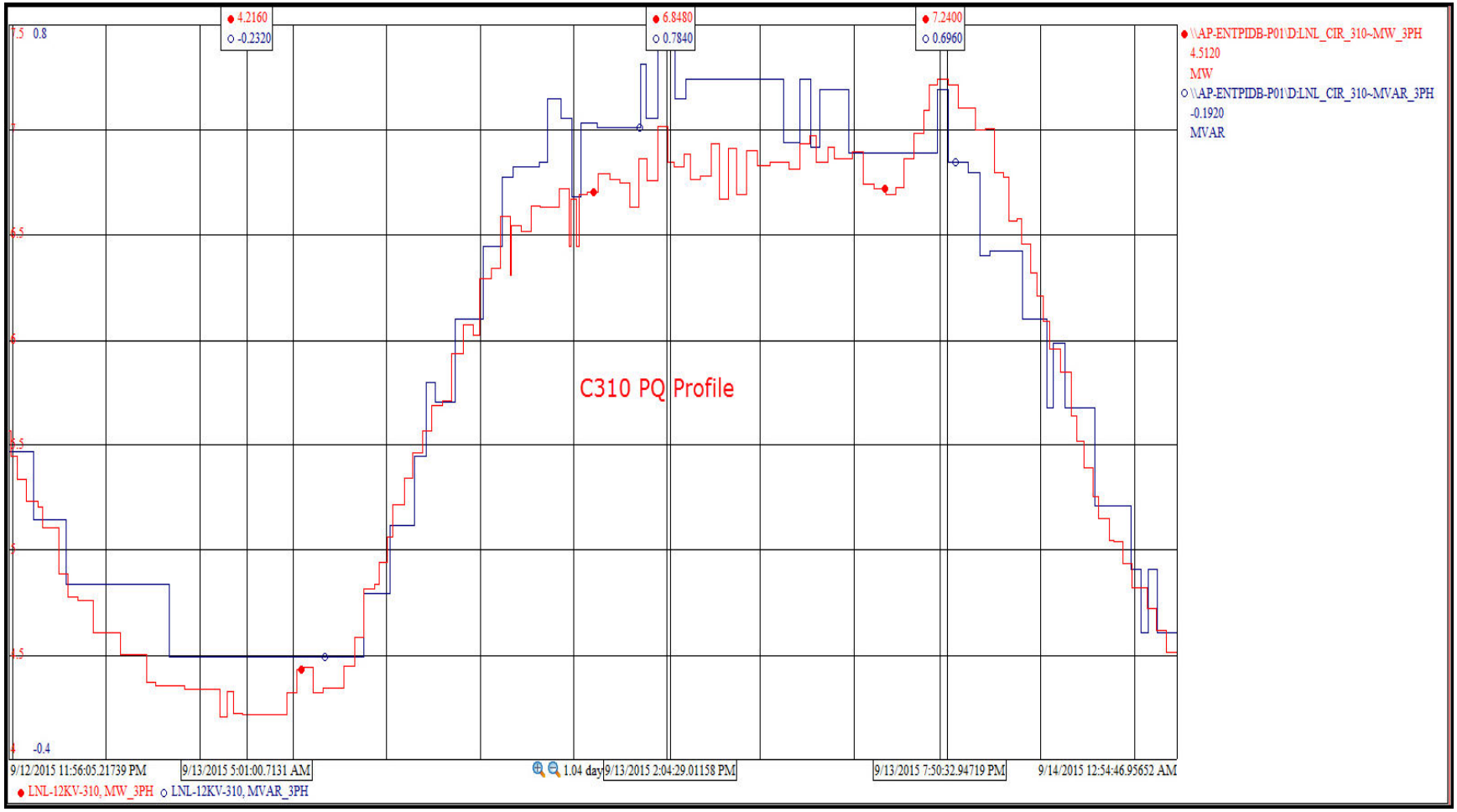

Figure B.1: Coastal-Residential Test Circuit – Actual Load Profile Over 24 Hours

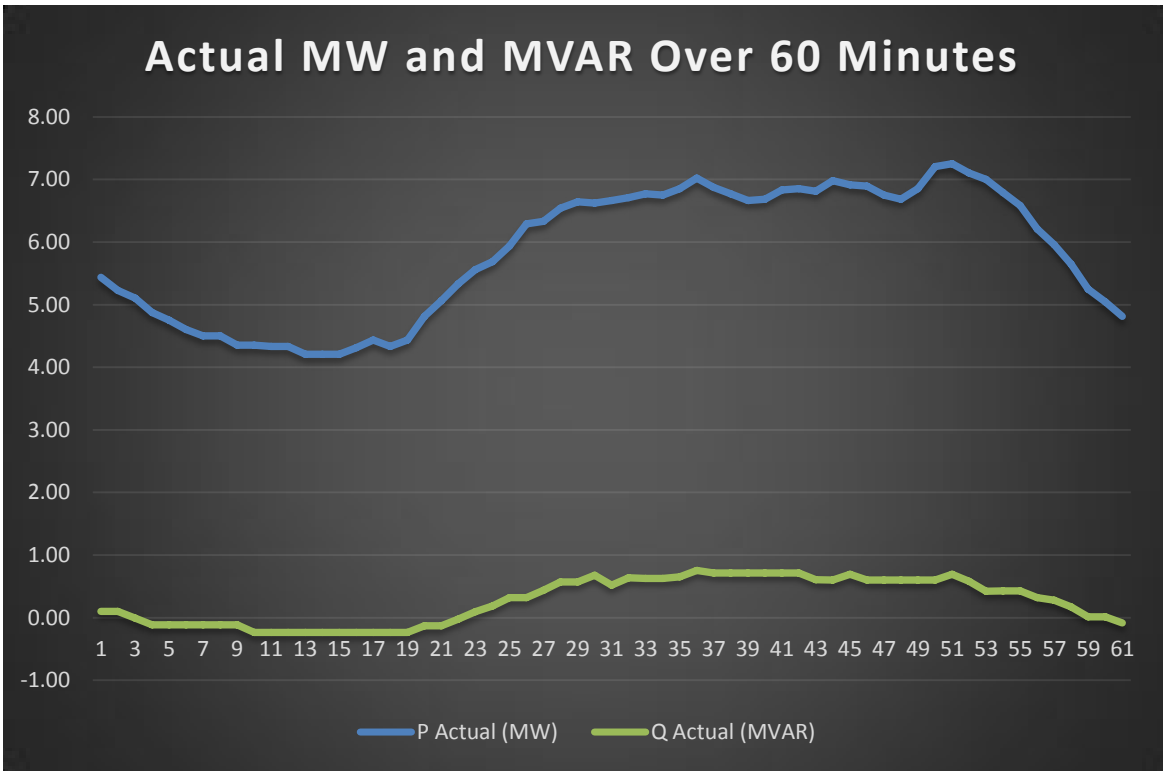

Figure B.2: Coastal-Residential Test Circuit – Actual Load Profile Over 60 Minutes

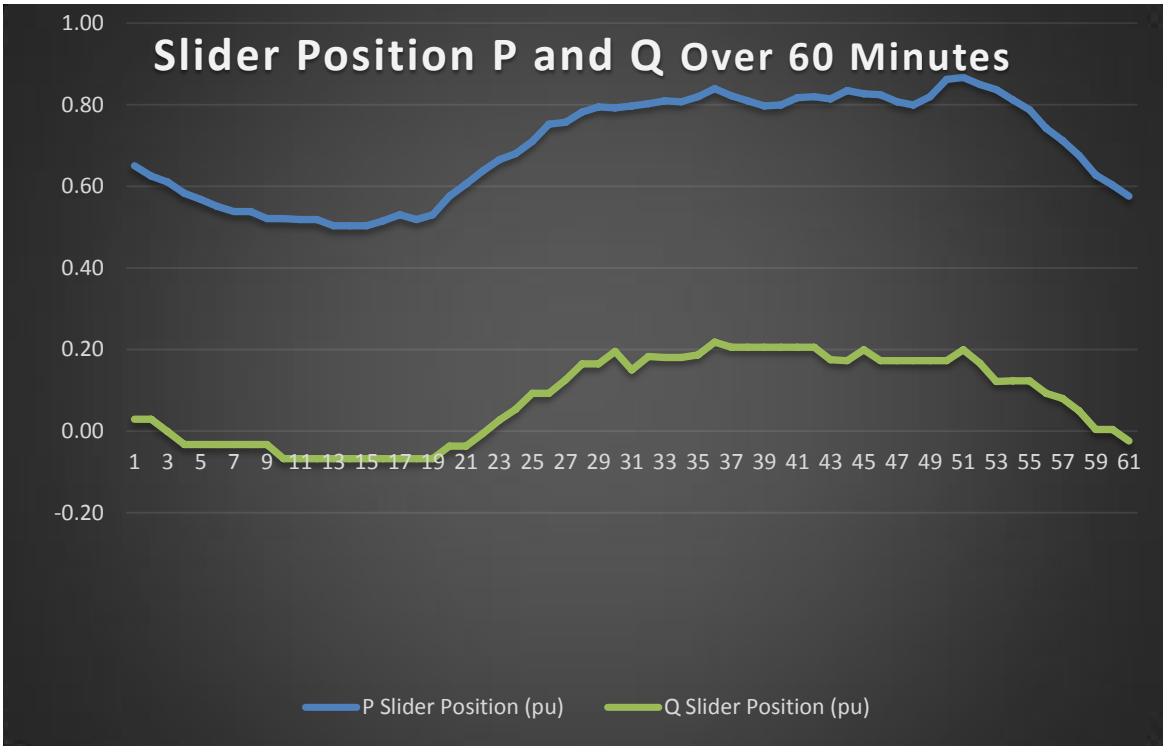

Figure B.3: Coastal-Residential Test Circuit – Slider Position Over 60 Minutes

Table 16.1: Load and Slider Position Value – Coastal-Residential Test Circuit

Time	P Actual (MW)	P Slider Position (pu)	Q Actual (MVAR)	Q Slider Position (pu)
1	5.44	0.65	0.100	0.029
2	5.23	0.63	0.100	0.029
3	5.10	0.61	–0.007	–0.002
4	4.88	0.58	–0.114	–0.033
5	4.75	0.57	–0.114	–0.033
6	4.60	0.55	–0.114	–0.033
7	4.50	0.54	–0.114	–0.033
8	4.50	0.54	–0.114	–0.033
9	4.35	0.52	–0.114	–0.033
10	4.35	0.52	–0.236	–0.068
11	4.33	0.52	–0.236	–0.068
12	4.33	0.52	–0.236	–0.068
13	4.21	0.50	–0.236	–0.068
14	4.21	0.50	–0.236	–0.068
15	4.21	0.50	–0.236	–0.068
16	4.31	0.52	–0.236	–0.068
17	4.44	0.53	–0.236	–0.068
18	4.33	0.52	–0.236	–0.068
19	4.44	0.53	–0.236	–0.068
20	4.81	0.58	–0.129	–0.037
21	5.06	0.61	–0.129	–0.037
22	5.33	0.64	–0.021	–0.006
23	5.56	0.66	0.093	0.027
24	5.69	0.68	0.186	0.053
25	5.94	0.71	0.321	0.092
26	6.29	0.75	0.321	0.092
27	6.33	0.76	0.436	0.125
28	6.54	0.78	0.571	0.164
29	6.65	0.79	0.571	0.164
30	6.63	0.79	0.679	0.195
31	6.67	0.80	0.521	0.150
32	6.71	0.80	0.636	0.183
33	6.77	0.81	0.629	0.181
34	6.75	0.81	0.629	0.181
35	6.85	0.82	0.650	0.187
36	7.02	0.84	0.757	0.218

Time	P Actual (MW)	P Slider Position (pu)	Q Actual (MVAR)	Q Slider Position (pu)
37	6.88	0.82	0.714	0.205
38	6.77	0.81	0.714	0.205
39	6.67	0.80	0.714	0.205
40	6.69	0.80	0.714	0.205
41	6.83	0.82	0.714	0.205
42	6.85	0.82	0.714	0.205
43	6.81	0.81	0.607	0.175
44	6.98	0.83	0.600	0.172
45	6.92	0.83	0.693	0.199
46	6.90	0.82	0.600	0.172
47	6.75	0.81	0.600	0.172
48	6.69	0.80	0.600	0.172
49	6.85	0.82	0.600	0.172
50	7.21	0.86	0.600	0.172
51	7.25	0.87	0.693	0.199
52	7.10	0.85	0.579	0.166
53	7.00	0.84	0.421	0.121
54	6.79	0.81	0.429	0.123
55	6.58	0.79	0.429	0.123
56	6.21	0.74	0.321	0.092
57	5.96	0.71	0.279	0.080
58	5.65	0.67	0.171	0.049
59	5.25	0.63	0.014	0.004
60	5.04	0.60	0.014	0.004
61	4.81	0.58	–0.086	–0.025

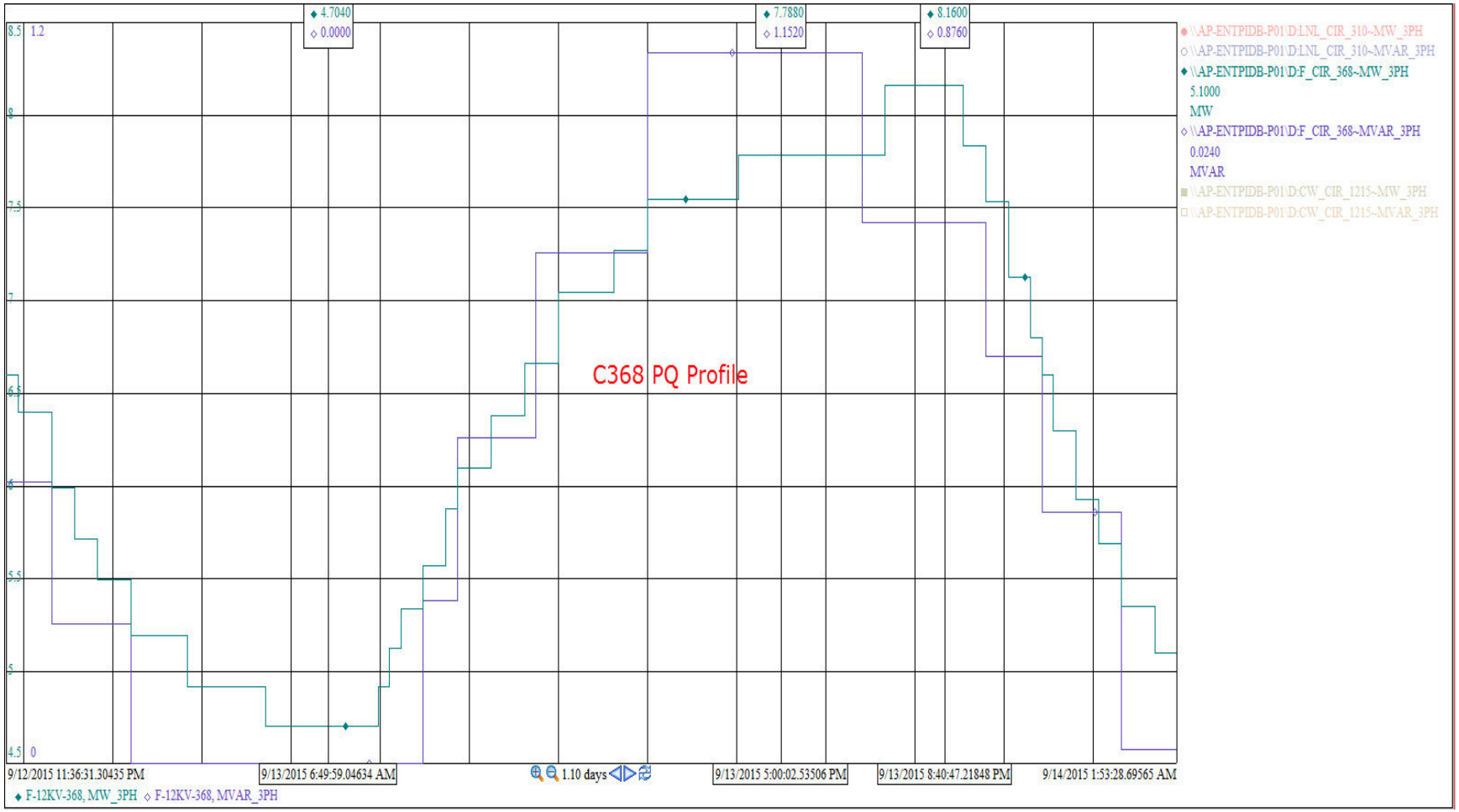

Figure B.4: Urban Test Circuit – Actual Load Profile Over 24 Hours

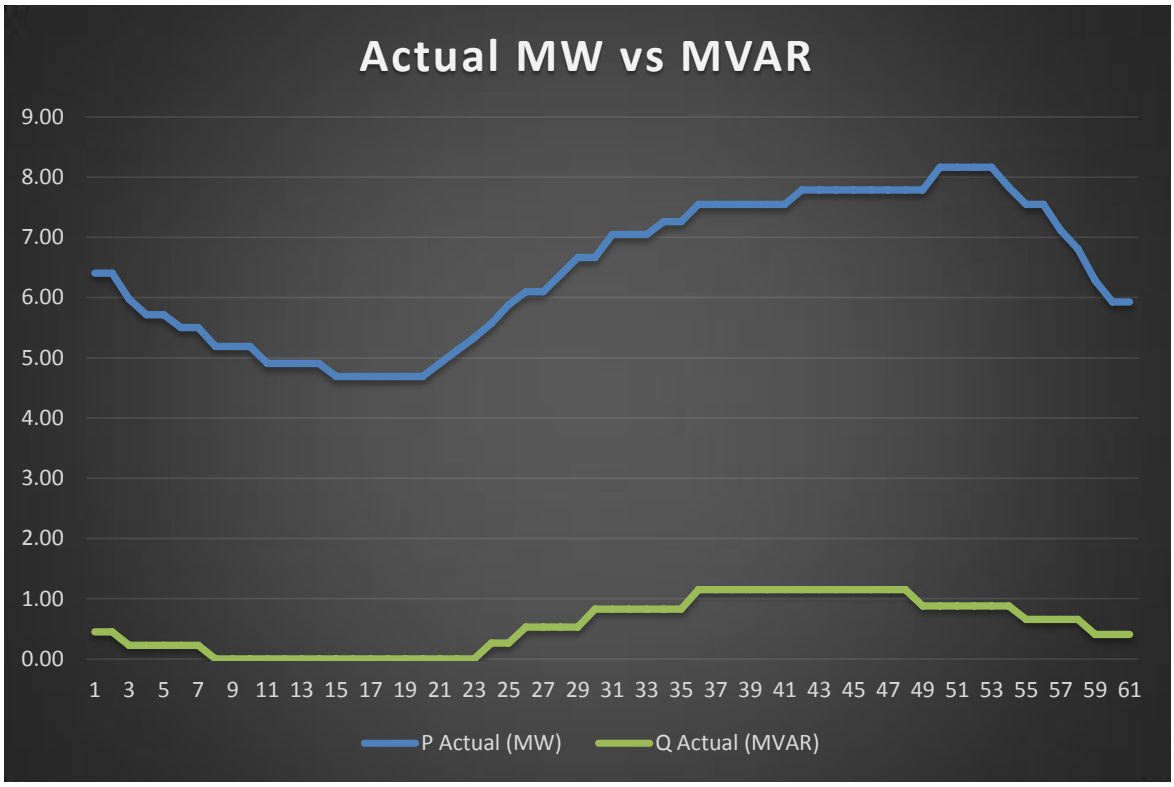

Figure B.5: Urban Test Circuit – Actual Load Profile Over 60 Minutes

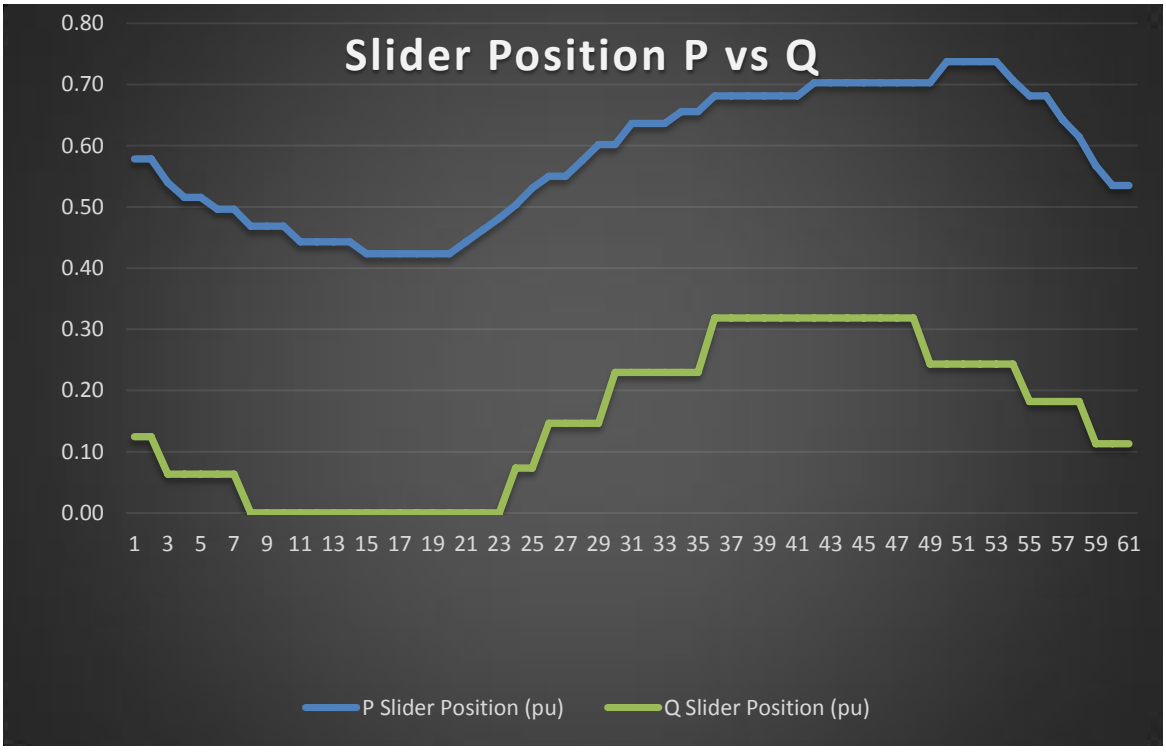

Figure B.6: Urban Test Circuit – Slider Position Over 60 Minutes

Table 16.2: Load and Slider Position Value – Urban Test Circuit

Time	P Actual (MW)	P Slider Position (pu)	Q Actual (MVAR)	Q Slider Position (pu)
1	6.40	0.58	0.450	0.125
2	6.40	0.58	0.450	0.125
3	5.98	0.54	0.229	0.063
4	5.71	0.52	0.229	0.063
5	5.71	0.52	0.229	0.063
6	5.50	0.50	0.229	0.063
7	5.50	0.50	0.229	0.063
8	5.19	0.47	0.000	0.000
9	5.19	0.47	0.000	0.000
10	5.19	0.47	0.000	0.000
11	4.90	0.44	0.000	0.000
12	4.90	0.44	0.000	0.000
13	4.90	0.44	0.000	0.000
14	4.90	0.44	0.000	0.000
15	4.69	0.42	0.000	0.000
16	4.69	0.42	0.000	0.000
17	4.69	0.42	0.000	0.000
18	4.69	0.42	0.000	0.000
19	4.69	0.42	0.000	0.000
20	4.69	0.42	0.000	0.000
21	4.90	0.44	0.000	0.000
22	5.12	0.46	0.000	0.000
23	5.33	0.48	0.000	0.000
24	5.57	0.50	0.264	0.073
25	5.88	0.53	0.264	0.073
26	6.10	0.55	0.529	0.146
27	6.10	0.55	0.529	0.146
28	6.38	0.58	0.529	0.146
29	6.67	0.60	0.529	0.146
30	6.67	0.60	0.829	0.229
31	7.05	0.64	0.829	0.229
32	7.05	0.64	0.829	0.229
33	7.05	0.64	0.829	0.229
34	7.26	0.66	0.829	0.229
35	7.26	0.66	0.829	0.229
36	7.55	0.68	1.150	0.318

Time	P Actual (MW)	P Slider Position (pu)	Q Actual (MVAR)	Q Slider Position (pu)
37	7.55	0.68	1.150	0.318
38	7.55	0.68	1.150	0.318
39	7.55	0.68	1.150	0.318
40	7.55	0.68	1.150	0.318
41	7.55	0.68	1.150	0.318
42	7.79	0.70	1.150	0.318
43	7.79	0.70	1.150	0.318
44	7.79	0.70	1.150	0.318
45	7.79	0.70	1.150	0.318
46	7.79	0.70	1.150	0.318
47	7.79	0.70	1.150	0.318
48	7.79	0.70	1.150	0.318
49	7.79	0.70	0.879	0.243
50	8.17	0.74	0.879	0.243
51	8.17	0.74	0.879	0.243
52	8.17	0.74	0.879	0.243
53	8.17	0.74	0.879	0.243
54	7.83	0.71	0.879	0.243
55	7.55	0.68	0.657	0.182
56	7.55	0.68	0.657	0.182
57	7.12	0.64	0.657	0.182
58	6.81	0.61	0.657	0.182
59	6.29	0.57	0.407	0.113
60	5.93	0.54	0.407	0.113
61	5.93	0.54	0.407	0.113

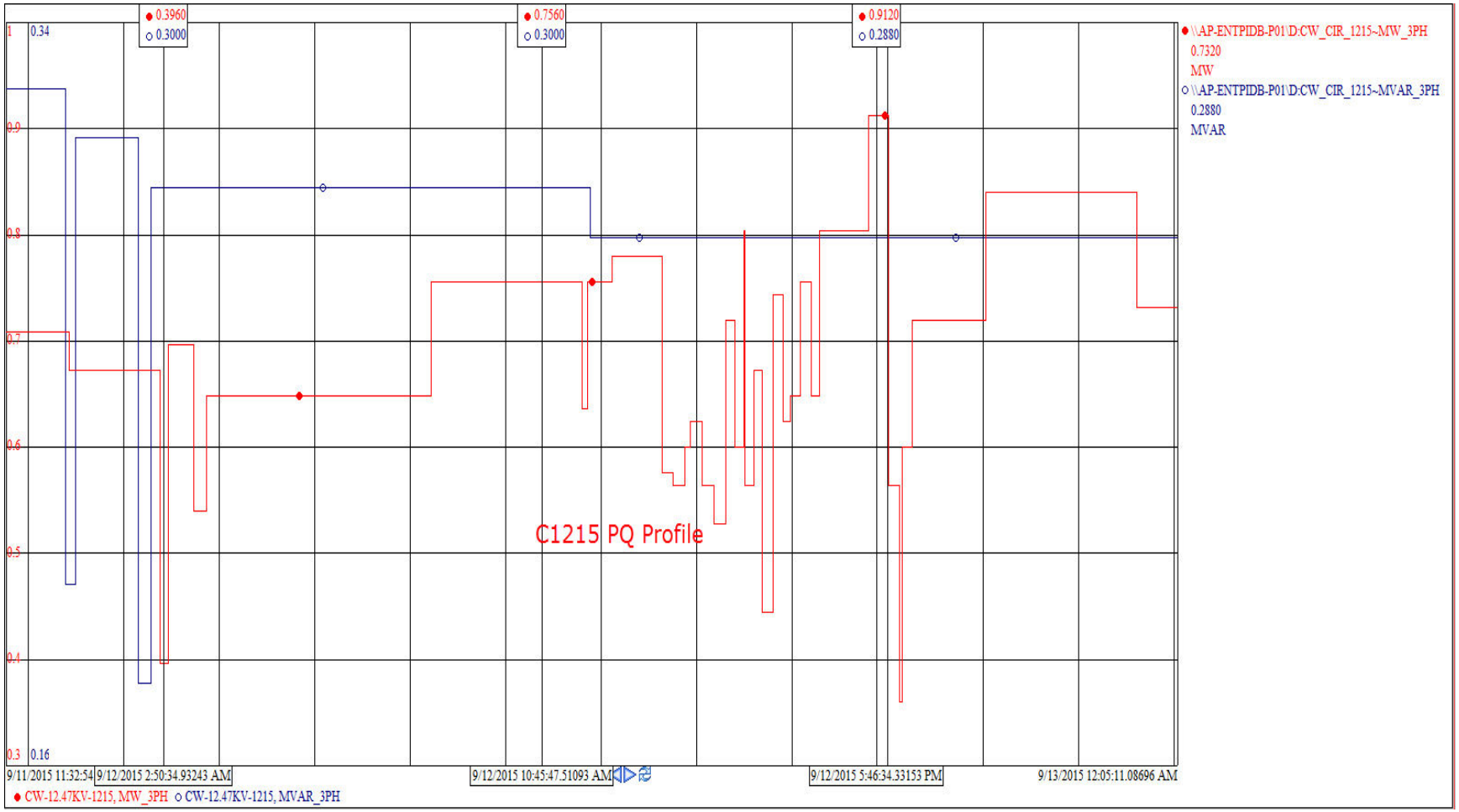

Figure B.7: Desert-Rural Test Circuit – Actual Load Profile Over 24 Hours

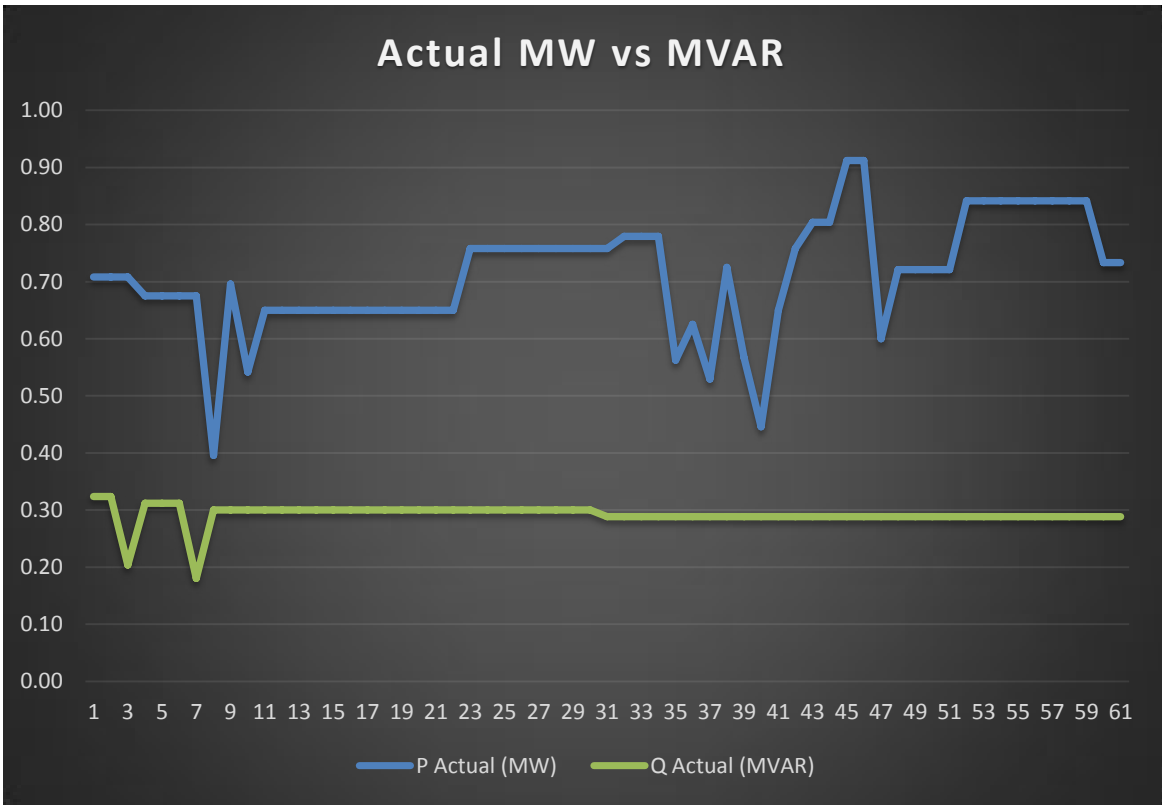

Figure B.8: Desert-Rural Test Circuit – Actual Load Profile Over 60 Minutes

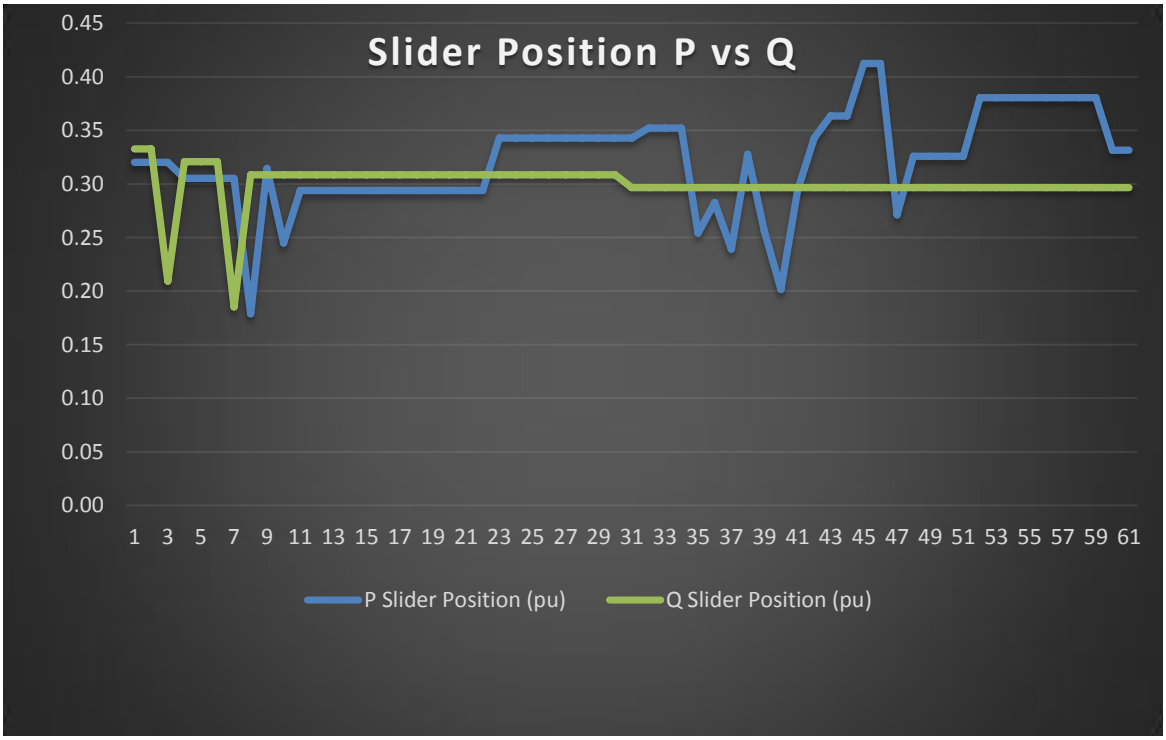

Figure B.9: Desert-Rural Test Circuit – Slider Position Over 60 Minutes

Table 16.3: Load and Slider Position Value – Desert-Rural Test Circuit

Time	P Actual (MW)	P Slider Position (pu)	Q Actual (MVAR)	Q Slider Position (pu)
1	0.71	0.32	0.324	0.333
2	0.71	0.32	0.324	0.333
3	0.71	0.32	0.204	0.210
4	0.68	0.31	0.312	0.321
5	0.68	0.31	0.312	0.321
6	0.68	0.31	0.312	0.321
7	0.68	0.31	0.180	0.185
8	0.40	0.18	0.300	0.309
9	0.70	0.31	0.300	0.309
10	0.54	0.24	0.300	0.309
11	0.65	0.29	0.300	0.309
12	0.65	0.29	0.300	0.309
13	0.65	0.29	0.300	0.309
14	0.65	0.29	0.300	0.309
15	0.65	0.29	0.300	0.309
16	0.65	0.29	0.300	0.309
17	0.65	0.29	0.300	0.309
18	0.65	0.29	0.300	0.309
19	0.65	0.29	0.300	0.309
20	0.65	0.29	0.300	0.309
21	0.65	0.29	0.300	0.309
22	0.65	0.29	0.300	0.309
23	0.76	0.34	0.300	0.309
24	0.76	0.34	0.300	0.309
25	0.76	0.34	0.300	0.309
26	0.76	0.34	0.300	0.309
27	0.76	0.34	0.300	0.309
28	0.76	0.34	0.300	0.309
29	0.76	0.34	0.300	0.309
30	0.76	0.34	0.300	0.309
31	0.76	0.34	0.289	0.296
32	0.78	0.35	0.289	0.296
33	0.78	0.35	0.289	0.296
34	0.78	0.35	0.289	0.296
35	0.56	0.25	0.289	0.296
36	0.63	0.28	0.289	0.296

Time	P Actual (MW)	P Slider Position (pu)	Q Actual (MVAR)	Q Slider Position (pu)
37	0.53	0.24	0.289	0.296
38	0.73	0.33	0.289	0.296
39	0.57	0.26	0.289	0.296
40	0.45	0.20	0.289	0.296
41	0.65	0.29	0.289	0.296
42	0.76	0.34	0.289	0.296
43	0.80	0.36	0.289	0.296
44	0.80	0.36	0.289	0.296
45	0.91	0.41	0.289	0.296
46	0.91	0.41	0.289	0.296
47	0.60	0.27	0.289	0.296
48	0.72	0.33	0.289	0.296
49	0.72	0.33	0.289	0.296
50	0.72	0.33	0.289	0.296
51	0.72	0.33	0.289	0.296
52	0.84	0.38	0.289	0.296
53	0.84	0.38	0.289	0.296
54	0.84	0.38	0.289	0.296
55	0.84	0.38	0.289	0.296
56	0.84	0.38	0.289	0.296
57	0.84	0.38	0.289	0.296
58	0.84	0.38	0.289	0.296
59	0.84	0.38	0.289	0.296
60	0.73	0.33	0.289	0.296
61	0.73	0.33	0.289	0.296

APPENDIX C VOLTAGE REGULATOR CONTROL SETTINGS

This appendix includes the settings used for the laboratory demonstration of the stand-alone voltage regulator tests described in Section 6.

Settings Calculation Sheet for the Voltage Regulator Control

kVA := kV·A pu := 1

MVA := MW j := $\sqrt{-1}$

Regulator Nameplate Data:

Set the kV to the voltage regulator rated nameplate line-neutral voltage.

Regulator Rated Voltage Line to Neutral: KV := 7.2kV

Select the polarity of the current transformer (CT) connection.

Regulator CT Winding Polarity: CTPOL := "NORM"

Set the voltage regulator primary CT nominal rating in primary amps.

Regulator Primary Current: CTPRIM := 10A

Regulator CT Ratio: CTR := 60

Set the regulator type to the tap changer manufacturer.

Regulator Type: TAPCHNGR := "COOPER"

Set the tapchanger type.

Tap Changer Type: TYPE := "B"

Select the polarity of the potential transformer (PT) PT1 connection.

PT1 Winding Polarity: PT1POL := "NORM"

Enter the primary and secondary winding information for the PT1 source.

PT1 Primary Voltage: PT1PRIM := 7.20kV

PT1 Secondary Voltage: PT1SEC := 120V

If there is a second PT connected on the source or load side of the voltage regulator, enable the second PT.

Second PT Connected: _2ND_PT := "Y"

PT2 Winding Polarity: PT2POL := "NORM"

Regulator PT2 Primary Voltage: PT2PRIM := 7.20kV

Regulator PT2 Secondary Voltage: PT2SEC := 120V

Connection Data:

Set the nominal system primary line-to-neutral voltage, and the nominal secondary voltage.

Base Primary Voltage: $BASE_{pri} := 7.2kV$

Base Secondary Voltage: $BASE_{sec} := 120V$

Set the regulator secondary connection.

Regulator Configuration: $CONFIG := "WYE"$

Set the delta configuration to be an open or closed delta.

Delta Power Type: $DELTA := "CLOSED"$

Angle By Which I Lags V: $D\_LAG := 30deg$

Angle By Which I Leads V: $D\_LEAD := 30deg$

Angle By Which I Lags V: $ISHIFT := 0deg$

Configuration Settings:

X corresponds to the specific phase - A, B or C.

Terminal Identification: $TID := "1215\text{-}68GX"$

The operation of the voltage regulator has several automatic modes to accommodate different operating conditions and applications. The modes are LOCKFWD, LOCKREV, IDLEREV, BIDIR, and COGEN. The regulator is utilized to regulate the bus voltage for forward load flow. The operation mode will be set in the locked forward mode.

Operating Mode: $OPMODE := "LOCKFWD"$

The nominal load current measured by the regulator is calculated based on the transformer MVA rating.

$MVA_{SelfCool} := 7.5MVA$ $V_{W2} := 12.47kV$ $I_{W2} := \frac{MVA_{SelfCool}}{\sqrt{3} \cdot V_{W2}}$ $I_{W2} = 347.24A$

The TAPMAX and TAPMIN settings provide a software limit switch on the regulator. The maximum allowable setting is +/- 16, which corresponds to +/- 10% voltage regulation. If +/- 8 was used, it would correspond to +/- 5% voltage regulation. With the load nominal load current well below the regular rated current, the voltage regulation can be set to achieve maximum regulation.

Maximum Software Tap Number: $TAPMAX := 16$

Minimum Software Tap Number: $TAPMIN := -16$

After the first tap, if additional tapping is needed to bring the voltage back within its normal range, the timing reverts to setting TD2 (Time Delay for Subsequent Taps).

Time Delay 2 for Subsequent Taps: TD2 := 10s

Forward Controller Settings:

There are multiple modes for resetting. The FAST time characteristic is the basic method for resetting the first-tap definite time delay. The DISC characteristic operates on the traditional induction disc relay. The DELAY mode prevents the resetting when the regulated voltage momentarily goes back in band. The DLY_FRZ characteristic freezes the timer when the regulated voltage enters the in-band region.

Forward Reset Characteristic: F_CHAR := "DISC"

Forward Center Band: F_CNBND := 120V

Forward Band Width: F_BNDWD := 2.0V

Forward Time Delay 1 for First Tap: F_TD1 := 30.0s

Forward Disc-like Reset Factor: F_DISC := 0.60

Forward Delay on Reset: F_DLYRS := 0.0

Reverse Controller Settings:

There are multiple modes for resetting. The FAST time characteristic is the basic method for resetting the first-tap definite time delay. The DISC characteristic operates on the traditional induction disc relay. The DELAY mode prevents the resetting when the regulated voltage momentarily goes back in band. The DLY_FRZ characteristic freezes the timer when the regulated voltage enters the in-band region.

The Reverse Controller Settings have been disabled since the device is on "LOCKFWD" operation.

Reverse Reset Characteristic: R_CHAR := "DISC"

Reverse Center Band: R_CNBND := 120V

Reverse Band Width: R_BNDWD := 2.0V

Reverse Time Delay 1 for First Tap: R_TD1 := 30.0s

Reverse Disc-like Reset Factor: R_DISC := 0.60

Reverse Delay on Reset: R_DLYRS := 0.0

Line Drop Compensation Settings:

The Line Drop Compensation (LDC) Settings are used when the delivery point for regulated voltage is beyond the load terminal on the voltage regulator. Line drop compensation keeps the voltage constant at the delivery point.

Enable Line Drop Compensation: ELDC := "N"

Line Drop Compensation is disabled in this study.

Forward Resistive LDC Voltage: VLDCFWR := 0.0V

Forward Reactive LDC Voltage: VLDCFWX := 0.0V

Reverse Resistive LDC Voltage: VLDCRVR := 0.0V

Reverse Reactive LDC Voltage: VLDCRVX := 0.0V

Overcurrent Settings:

Seven levels of load overcurrent elements are available. There are also two directional threshold elements which are used to determine the operational mode of the voltage regulator control. One fast operating fault overcurrent element is provided to trigger an alarm when an overcurrent fault occurs on the power system.

Load Current Levels: E50L := "1"

The load overcurrent element is set to 125% of the rated regulator current and is used to block the voltage regulator control from changing taps when asserted and does not reset the regulation timers.

Load OC Setting: $_{50L1P} := \frac{150\% \cdot CTPRIM}{CTR}$ $_{50L1P} = 0.25A$

The fault overcurrent element is set to 200% of the rated regular current and is used to block the voltage regulator control from changing taps when asserted.

Fault OC Setting: $_{50FLTP} := \frac{200\% \cdot CTPRIM}{CTR}$ $_{50FLTP} = 0.33A$

Set the forward and reverse directional thresholds.

Forward I Threshold: _50FWDP := 0.002A

Reverse I Threshold: _50REVP := 0.002A

Voltage Reduction Settings:

Voltage reduction is the deliberate lowering of the system voltage when the power demand exceeds the supply. This reduction in voltage is achieved by lowering the existing center band setting by a predefined percentage.

Voltage reduction settings are disabled in this study.

Enable Voltage Reduction: ENREDUC := "N"

Voltage Reduction Mode: VREDMOD := "PULSE, LATCH, CONTROL"

Forward VR 1 Percent: VREDFP1 := 2.0

Reverse VR 1 Percent:	VREDRP1 := 2.0
VR Stage 1 Timer PU:	VRSPU1 := 2.0
VR Pulse Length Pulse Mode:	VRPULPU := 0.02
Set LDC to Zero for Voltage Reduction:	SETLDC0 := "Y, N"

Voltage Limit Settings:

The voltage regulator control causes a voltage regulator to automatically tap to keep the regulation point voltage within its range. Setting limits attempts to prevent the voltage regulator from automatically tapping too high or too low and causing abnormally high or low voltage at the voltage regulator location.

Enable Min/Max Voltage Control:	ENLIMIT := "Y"
Maximum Volts:	VMAX := 130.0V
Minimum Volts:	VMIN := 110.0V

Runback Settings:

Additional runback (high and low) limits will instigate automatic tapping to bring the voltage back within its normal range. These runback limits are outside the VMAX/VMIN limits based on the dead band high/low settings.

Runback settings are disabled in this study.

Enable Runback:	ENRUNBK := "N"
Runback Block:	RBKBLSV := "50FLT"
Runback Timer:	RUNBKPU := 0.5s
Dead Band (High):	DBNDH := OFF
Dead Band (Low):	DBNDL := OFF

Timer Settings:

The Timers provide additional settings functionality by adding state variables that can be manipulated.

Timers:	ESV := 2
Variable Input Equation:	SV01 = RSEFAIL OR LWRFAIL OR XTAP16R OR XTAP16L OR OPNOCUR OR TAP_DIF For interface error conditions
Variable Timer Pickup (seconds)	SV01PU := 0
Variable Timer Dropout (seconds)	SV01DO := 2.0

Variable Input Equation: SV02 = VLSI

For system low voltage, used in BLOCKSV

Variable Timer Pickup (seconds) SV02PU := 0

Variable Timer Dropout (seconds) SV02DO := 2.0

Raise/Lower Settings:

Inhibit Conditions:

INHIBSV := "50FLT"

Block Tap Operations:

BLOCKSV := "50L1 OR SV02T'

Raise Command:

RAISESV := "TOOLOW AND AUTO"

Lower Command:

LOWERSV := "TOOHIGH AND AUTO"

Output Equations:

OUT101 := "NOT ALARM"

OUT102 := "RAISE"

OUT103 := "LOWER"

OUT104 := "BLOCKSV"

APPENDIX D RECLOSER SETTINGS SHEET

This appendix documents the sample field settings provided by SDG&E for recloser controllers on the desert-rural test circuit. These settings were further modified for the high-impedance fault detection tests described in Section 8.

	PROFILE 1 NORMAL			PROFILE 2 INRUSH			PROFILE 3 FAST/SENSITIZED			PROFILE 4 SWITCH		
	1	Phase	Gnd		Phase	Gnd		Phase	Gnd		Phase	Gnd
Initial Trip Settings										All Protection Disabled		
Min Trip/Fault Ind Pick Up Amps	Enabled	150	100	Enabled	180	100	Enabled	100	25	Fault Ind	150	100
TCC for Initial, Test, & Closing Profiles		U3	U3		U3	U3		U3	U3			
Time Mult (Time Dial)		2.00	5.00		2.00	5.00		2.00	5.00			
Min TCC Response Time (sec)		0.05	0.05		0.05	0.05		0.05	0.05			
Time Adder		0	0		0	0		0	0			
Disc Reset Type (EM or DT)	E/M	calc	calc	E/M	calc	calc	E/M	calc	calc			
Low Cut-off (Amps)		N/A	N/A		N/A	N/A		N/A	N/A			
Initial Def Time-1		1300	1300		1300	1300		100	25			
Initial Def Time-1 Delay		0.050	0.050		0.050	0.050		0.050	0.050			
Initial Def Time-2		N/A	N/A		N/A	N/A		1300	1300			
Initial Def Time-2 Delay		0.000	0.000		0.000	0.000		0.000	0.000			
High Current Lockout Initial Trip	Disabled		1300	Enabled		1300	Enabled		1300			
Sensitive Earth	Enable			Enable			Enable					
TCC Minimum Trip (Amps)			20			20			20			
TCC Minimum Trip (Seconds)			2			2			2			
TCC			U1			U1			U1			
TCC Time Multiplier			15			15			15			
TCC Time Adder (Seconds)			0			0			0			
TCC Reset Time (Seconds)			120			120			120			
TCC Low Cut-off (Amps)			NA			NA			NA			
Def Time-1 Pick Up (Amps)			20			20			20			
Def Time-1 Min Trip (Seconds)			5.0			5			5			
SGF Number of Tests			0			0			0			
Reset			T/A			T/A			T/A			
SGF Spike Counting	Enable			Enable			Enable					
Number of Spikes	25			25			25					
Moving Reset Window (seconds)	40			40			40					
TCCs for Test Sequence 1 and 2												
All same as Initial Trip except:												
High Current Lockout Test 1 & 2:	Enabled		1300	Disabled			Disabled					
Testing After Intital Trip												
TCC Trips to lockout (see next line)	3			1			1					
High Current Operations to lockout	2			0			0					
Over-current Number of Tests	2			0			0					
Open Intervals (seconds)	5, 10			n/a			n/a					
Reset time (seconds)	120			n/a			n/a					
Hot Line Tag	GLOBAL			GLOBAL			GLOBAL					
TCC settings = Initial Trip EXCEPT:												
TCC		106	102									
Time Multiplier (Time Dial)		1.00	1.00									
Closing Profiles	GLOBAL			GLOBAL			GLOBAL					
Pulse 1- Test or Close	Pulse Close											
Profile1- Pulse Closing Enabled	Yes											
Pulse 2- Test or Close	Non-Pulse											
Profile2- Pulse Closing Enabled	No											
Profile Active Time (Seconds)	1											
External Lever Delay (Seconds)	2											
Sync Check Enabled	No											
TCC settings = Initial Trip EXCEPT:												
Min Trip Amps (Double Phase Amps)		300	300									
Cold Load Pick Up	GLOBAL			GLOBAL			GLOBAL					
Activate Cold Load Pick-up	Enabled											
Max Cold Load Modifier (%)	120%	180			216			120				
T1-Apply Delay (Minutes)	15											
T2-Ramp-up Delay (Minutes)	15											
T3-Ramp-down Delay (Minutes)	15											
T4-Removal Delay (Minutes)	15											

Normal Curve Setting Pick Up Times	Phase Curve Testing						Ground Curve Testing					
	Min PU	Curve	TD/Mult	200%	500%	1000%	Min PU	Curve	TD/Mult	200%	500%	1000%
Settings and ASPEN pickup times (sec):	150	U3	2.00	2.779	0.516	0.271	100	U3	5.00	6.948	1.290	0.677
Field test times (sec):												

TESTING NOTES:

	PROFILE 1 NORMAL			PROFILE 2 INRUSH			PROFILE 3 FAST/SENSITIZED			PROFILE 4 SWITCH		
	1	Phase	Gnd		Phase	Gnd		Phase	Gnd		Phase	Gnd
Initial Trip Settings										All Protection Disabled		
Min Trip/Fault Ind Pick Up Amps	Enabled	**180**	**130**	Enabled	**220**	**130**	Enabled	**100**	**30**	Fault Ind	**180**	**130**
TCC for Initial, Test, & Closing Profiles		U3	U4		U3	U4		U3	U4			
Time Mult (Time Dial)		4.30	6.30		4.30	6.30		4.30	6.30			
Min TCC Response Time (sec)		0.05	0.05		0.05	0.05		0.05	0.05			
Time Adder		0	0		0	0		0	0			
Disc Reset Type (EM or DT)	E/M	calc	calc	E/M	calc	calc	E/M	calc	calc			
Low Cut-off (Amps)		N/A	N/A		N/A	N/A		N/A	N/A			
Initial Def Time-1		1500	1500		1500	1500		100	30			
Initial Def Time-1 Delay		0.050	0.050		0.050	0.050		0.050	0.050			
Initial Def Time-2		N/A	N/A		N/A	N/A		1500	1500			
Initial Def Time-2 Delay		0.000	0.000		0.000	0.000		0.000	0.000			
High Current Lockout Initial Trip	Disabled		1500	Enabled		1500	Enabled		1500			
Sensitive Earth	Enable			Enable			Enable					
TCC Minimum Trip (Amps)			25			25			25			
TCC Minimum Trip (Seconds)			2			2			2			
TCC			U1			U1			U1			
TCC Time Multiplier			15			15			15			
TCC Time Adder (Seconds)			0			0			0			
TCC Reset Time (Seconds)			120			120			120			
TCC Low Cut-off (Amps)			NA			NA			NA			
Def Time-1 Pick Up (Amps)			25			25			25			
Def Time-1 Min Trip (Seconds)			5.0			5			5			
SGF Number of Tests			0			0			0			
Reset			T/A			T/A			T/A			
SGF Spike Counting	Enable			Enable			Enable					
Number of Spikes	25			25			25					
Moving Reset Window (seconds)	40			40			40					
TCCs for Test Sequence 1 and 2												
All same as Initial Trip except:												
High Current Lockout Test 1 & 2:	Enabled		1500	Disabled			Disabled					
Testing After Intital Trip												
TCC Trips to lockout (see next line)	3			1			1					
High Current Operations to lockout	2			0			0					
Over-current Number of Tests	2			0			0					
Open Intervals (seconds)	5, 10			n/a			n/a					
Reset time (seconds)	120			n/a			n/a					
Hot Line Tag	GLOBAL			GLOBAL			GLOBAL					
TCC settings = Initial Trip EXCEPT:												
TCC		**106**	**102**									
Time Multiplier (Time Dial)		**1.00**	**1.00**									
Closing Profiles	GLOBAL			GLOBAL			GLOBAL					
Pulse 1- Test or Close	Pulse Close											
Profile1- Pulse Closing Enabled	Yes											
Pulse 2- Test or Close	Non-Pulse											
Profile2- Pulse Closing Enabled	No											
Profile Active Time (Seconds)	1											
External Lever Delay (Seconds)	2											
Sync Check Enabled	No											
TCC settings = Initial Trip EXCEPT:												
Min Trip Amps (Double Phase Amps)		**360**	**360**									
Cold Load Pick Up	GLOBAL			GLOBAL			GLOBAL					
Activate Cold Load Pick-up	Enabled											
Max Cold Load Modifier (%)	120%	**216**			**264**			**120**				
T1-Apply Delay (Minutes)	15											
T2-Ramp-up Delay (Minutes)	15											
T3-Ramp-down Delay (Minutes)	15											
T4-Removal Delay (Minutes)	15											

Normal Curve Setting Pick Up Times	**Phase Curve Testing**						**Ground Curve Testing**					
	Min PU	Curve	TD/Mult	200%	500%	1000%	Min PU	Curve	TD/Mult	200%	500%	1000%
Settings and ASPEN pickup times (sec):	180	U3	4.30	5.975	1.109	0.583	130	U4	6.30	12.129	1.710	0.583
Field test times (sec):												

TESTING NOTES:

	PROFILE 1			PROFILE 2			PROFILE 3			PROFILE 4		
	NORMAL			INRUSH			FAST/SENSITIZED			SWITCH		
	1	Phase	Gnd		Phase	Gnd		Phase	Gnd		Phase	Gnd
Initial Trip Settings										All Protection Disabled		
Min Trip/Fault Ind Pick Up Amps	Enabled	**125**	**100**	Enabled	**150**	**100**	Enabled	**100**	**25**	Fault Ind	**125**	**100**
TCC for Initial, Test, & Closing Profiles		U3	U4		U3	U4		U3	U4			
Time Mult (Time Dial)		3.40	4.30		3.40	4.30		3.40	4.30			
Min TCC Response Time (sec)		0.05	0.05		0.05	0.05		0.05	0.05			
Time Adder		0	0		0	0		0	0			
Disc Reset Type (EM or DT)	E/M	calc	calc	E/M	calc	calc	E/M	calc	calc			
Low Cut-off (Amps)		N/A	N/A		N/A	N/A		N/A	N/A			
Initial Def Time-1		1300	1300		1300	1300		100	25			
Initial Def Time-1 Delay		0.050	0.050		0.050	0.050		0.050	0.050			
Initial Def Time-2		N/A	N/A		N/A	N/A		1300	1300			
Initial Def Time-2 Delay		0.000	0.000		0.000	0.000		0.000	0.000			
High Current Lockout Initial Trip	Disabled		1300	Enabled		1300	Enabled		1300			
Sensitive Earth	Enable			Enable			Enable					
TCC Minimum Trip (Amps)			20			20			20			
TCC Minimum Trip (Seconds)			2			2			2			
TCC			U1			U1			U1			
TCC Time Multiplier			15			15			15			
TCC Time Adder (Seconds)			0			0			0			
TCC Reset Time (Seconds)			120			120			120			
TCC Low Cut-off (Amps)			NA			NA			NA			
Def Time-1 Pick Up (Amps)			20			20			20			
Def Time-1 Min Trip (Seconds)			4.5			4.5			4.5			
SGF Number of Tests			0			0			0			
Reset			T/A			T/A			T/A			
SGF Spike Counting	Enable			Enable			Enable					
Number of Spikes	25			25			25					
Moving Reset Window (seconds)	40			40			40					
TCCs for Test Sequence 1 and 2												
All same as Initial Trip except:												
High Current Lockout Test 1 & 2:	Enabled		1300	Disabled			Disabled					
Testing After Intital Trip												
TCC Trips to lockout (see next line)	3			1			1					
High Current Operations to lockout	2			0			0					
Over-current Number of Tests	2			0			0					
Open Intervals (seconds)	5, 10			n/a			n/a					
Reset time (seconds)	120			n/a			n/a					
Hot Line Tag	GLOBAL			GLOBAL			GLOBAL					
TCC settings = Initial Trip EXCEPT:												
TCC		**106**	**102**									
Time Multiplier (Time Dial)		**1.00**	**1.00**									
Closing Profiles	GLOBAL			GLOBAL			GLOBAL					
Pulse 1- Test or Close	Pulse Close											
Profile1- Pulse Closing Enabled	Yes											
Pulse 2- Test or Close	Non-Pulse											
Profile2- Pulse Closing Enabled	No											
Profile Active Time (Seconds)	1											
External Lever Delay (Seconds)	2											
Sync Check Enabled	No											
TCC settings = Initial Trip EXCEPT:												
Min Trip Amps (Double Phase Amps)		**250**	**250**									
Cold Load Pick Up	GLOBAL			GLOBAL			GLOBAL					
Activate Cold Load Pick-up	Enabled											
Max Cold Load Modifier (%)	120%	**150**			**180**			**120**				
T1-Apply Delay (Minutes)	15											
T2-Ramp-up Delay (Minutes)	15											
T3-Ramp-down Delay (Minutes)	15											
T4-Removal Delay (Minutes)	15											

Normal Curve Setting Pick Up Times	Phase Curve Testing						Ground Curve Testing					
	Min PU	Curve	TD/Mult	200%	500%	1000%	Min PU	Curve	TD/Mult	200%	500%	1000%
Settings and ASPEN pickup times (sec):	125	U3	3.40	4.725	0.877	0.461	100	U4	4.30	8.278	1.167	0.398
Field test times (sec):												

TESTING NOTES:

	NORMAL			INRUSH RESTRAINT (CLPU TCCs)			PROFILE 3 (FAST/SENSITIZED)			SWITCH		
		Phase	Gnd		Phase	Gnd		Phase	Gnd		Phase	Gnd
Min Trip										Disabled		
Min Trip Pick Up		75	75		100	75		100	55			
Operations to lockout		3	3		1	1		1	1			
Block TCC Trips (F6 only: unblk/blk)		unblk	unblk		unblk	unblk		unblk	unblk		blk	blk
TCC1,2,3,4		151	142		151	142		151	142			
Min Response Time		0.05	0.05		0.05	0.05		0.05	0.05			
TCC Time Mult (F6only,1.0 if disabld)		0.50	0.50		0.50	0.50		0.50	0.50			
Open Intervals		5, 10,	5, 10,		5, 10,	5, 10,		5, 10,	5, 10,			
High Current Trip										Disabled		
Trip Delay, seconds		0.05	0.05		0.05	0.05		0.01	0.01			
Min Trip Pick Up (internal calc)	Enabled	1000	1000	Enabled	1000	1000	Enabled	1000	1000			
IT/PU Multiplier		13.33	13.33		10.00	13.33		10.00	18.18			
High Current Lockout										Disabled		
1st	Disabled			Enabled	1000	1000	Enabled	1000	1000			
2nd	Enabled	1000	1000	Disabled			Disabled					
3rd	Disabled			Disabled			Disabled					
Cold Load Pick Up	Enabled			Enabled			Enabled			Disabled		
Trips to lockout	2			1			1					
Activation time	20			20			20					
Open interval	2			2			2					
CLPU Min Pickup		100	75		100	75		100	75			
CLPU TCC		151	142		151	142		151	142			
Min Response Time		0.05	0.05		0.05	0.05		0.05	0.05			
CLPU TCC TimeMult (1.0 if disabld)		0.50	0.50		0.50	0.50		0.50	0.50			
High Current Lockout	Enabled			Enabled			Enabled					
HCL Threshold		1000	1000		1000	1000		1000	1000			
IT/PU Multiplier		10.00	13.33		10.00	13.33		10.00	13.33			
CLPU HCT Delay (sec)		0.050	0.050		0.050	0.050		0.050	0.050			
Disc Reset Coeff. (EM emulation)		4.00	4.00		4.00	4.00		4.00	4.00			
Sensitive Ground Fault	Enabled			Enabled			Enabled			Disabled		
Minimum Trip	50			50			50					
Trip Delay, seconds	4.0			4			4					
Open Intervals, seconds	2			2			2					
Operations to lockout	1			1			1					
Reset Delay, seconds	60			60			60					
Downed Cond Detection (DCD)	Enabled			Enabled			Enabled			Disabled		
DCD Spike Accum: Counts (N) / Sec (W)	15, 120			15, 120			15, 120					
DCD Spike Pick Up Buffer (amps)	25			25			25					
DCD IN (60HZ) Accum: Counts (N) / Sec (W)	15, 120			15, 120			15, 120					
DCD IN (60HZ) Pick Up Buffer (amps)	13			13			13					
DCD Counter Alarm (max before alarms)	5			5			5					
DCD SEF Adapt INT (min) / K(multipier)	1, 1			1, 1			1, 1					
DCD Run Accum (amps) / SEF Bolted (sec)	3, 1			3, 1			3, 1					
Low Set Trip (Form 6 only)	Disabled			Disabled			Enabled			Disabled		
Amps								100	55			
Delay, seconds								0.05	0.05			
Hot Line Tag	Enabled			Enabled			Enabled			Disabled		
Profile Min Trip (internal setting)		75	75		100	75		100	55			
Delay before trip		0.05	0.05		0.05	0.05		0.05	0.05			

Normal Curve Setting Pick Up Times	**Phase Curve Testing**						**Ground Curve Testing**					
	Min PU	Curve	TD/Mult	200%	500%	1000%	Min PU	Curve	TD/Mult	200%	500%	1000%
Settings and ASPEN pickup times (sec):	75	151	0.50	3.098	0.562	0.294	75	142	0.50	4.850	0.435	0.123
Field test times (sec):												

TESTING NOTES: **On return to service, field tech to take snapshots of Low & High harmonic screens and email to Syst Prot Eng.**